UC1842, UC2842, UC3842, UC1843, UC2843, UC3843
UC1844, UC2844, UC3844, UC1845, UC2845, UC3845
SLUS223F – APRIL 1997 – REVISED APRIL 2020

UCx84x Current-Mode PWM Controllers

1 Features

- Optimized for off-line and DC-to-DC converters
- Low start-up current (< 1 mA)
- Automatic feedforward compensation
- Pulse-by-pulse current limiting
- Enhanced load-response characteristics
- Undervoltage lockout with hysteresis
- Double-pulse suppression
- High-current totem-pole output
- Internally trimmed bandgap reference
- Up to 500-kHz operation
- Error amplifier with low output resistance

2 Applications

- Switching regulators of any polarity
- Transformer-coupled DC-DC converters

3 Description

The UCx84x series of control integrated circuits provide the features that are necessary to implement off-line or DC-to-DC fixed-frequency current-mode control schemes, with a minimum number of external components. The internally implemented circuits include an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and a totem-pole output stage that is designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

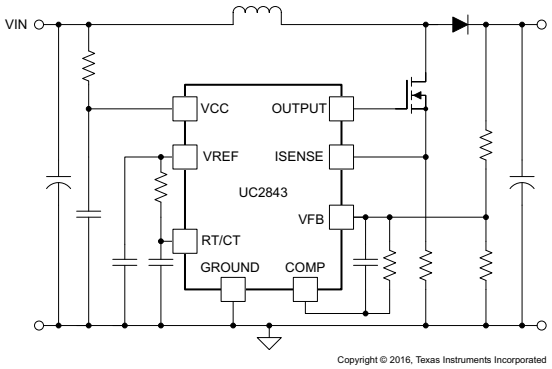
The UCx84x family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of turnon and turnoff thresholds and hysteresis ranges. Devices with higher turnon or turnoff hysteresis are ideal choices for off-line power supplies, while the devices with a narrower hysteresis range are suited for DC-DC applications. The UC184x devices are specified for operation from –55°C to 125°C, the UC284x series is specified for operation from –40°C to 85°C, and the UC384x series is specified for operation from 0°C to 70°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
UC184x	CDIP (8)	9.60 mm × 6.67 mm
	LCCC (20)	8.89 mm × 8.89 mm
	CFP (8)	9.21 mm × 5.97 mm
UC284x	SOIC (8)	4.90 mm × 3.91 mm
	SOIC (14)	8.65 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
UC384x	SOIC (8)	4.90 mm × 3.91 mm
	SOIC (14)	8.65 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	CFP (8)	9.21 mm × 5.97 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2017) to Revision F — **Page**

- Changed UVLO Table updated ... 8

Changes from Revision D (August 2016) to Revision E — **Page**

- Changed $V_{REFLECTED}$ equation. ... 23
- Changed D_{MAX} equation. ... 24

Changes from Revision C (June 2007) to Revision D — **Page**

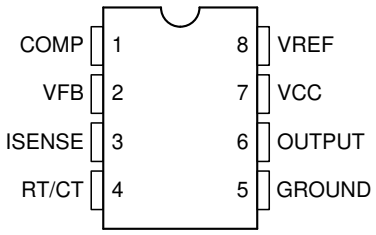
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed values in the *Thermal Information* table ... 6

5 Device Comparison Table

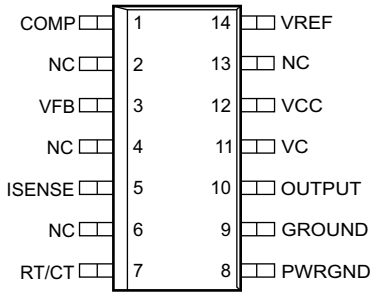
UVLO		TEMPERATURE RANGE	MAX DUTY CYCLE
TURNON AT 16 V TURNOFF AT 10 V SUITABLE FOR OFF-LINE APPLICATIONS	TURNON AT 8.4 V TURNOFF AT 7.6 V SUITABLE FOR DC-DC APPLICATIONS		
UC1842	UC1843	–55°C to 125°C	Up to 100%
UC2842	UC2843	–40°C to 85°C	
UC3842	UC3843	0°C to 70°C	
UC1844	UC1845	–55°C to 125°C	Up to 50%
UC2844	UC2845	–40°C to 85°C	
UC3844	UC3845	0°C to 70°C	

6 Pin Configuration and Functions

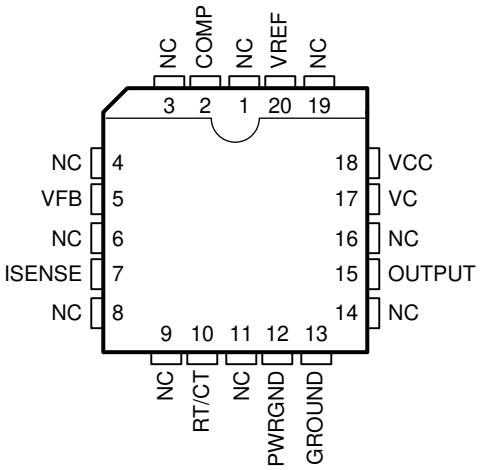
D, JG, and P Packages
8-Pin SOIC, CDIP, and PDIP
Top View



D and W Packages
14-Pin SOIC and CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	SOIC, CDIP, PDIP (8)	SOIC, CFP (14)	LCCC (20)		
COMP	1	1	2	O	Error amplifier compensation pin. Connect external compensation components to this pin to modify the error amplifier output. The error amplifier is internally current-limited so the user can command zero duty cycle by externally forcing COMP to GROUND.
GROUND	5	9	13	G	Analog ground. For device packages without PWRGND, GROUND functions as both power ground and analog ground.
PWRGND	—	8	12	G	Power ground. For device packages without PWRGND, GROUND functions as both power ground and analog ground
ISENSE	3	5	7	I	Primary-side current sense pin. Connect to current sensing resistor. The PWM uses this signal to terminate the OUTPUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage-mode control configuration.
NC	—	2, 4, 6, 13	1, 3, 4, 6, 8, 9, 11, 14, 16, 19	—	Do not connect
OUTPUT	6	10	15	O	OUTPUT is the gate drive for the external MOSFET. OUTPUT is the output of the on-chip driver stage intended to directly drive a MOSFET. Peak currents of up to 1 A are sourced and sunk by this pin. OUTPUT is actively held low when VCC is below the turnon threshold.
RT/CT	4	7	10	I/O	Fixed frequency oscillator set point. Connect timing resistor, R_{RT}, to VREF and timing capacitor, C_{CT}, to GROUND from this pin to set the switching frequency. For best performance, keep the timing capacitor lead to the device GROUND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions. The frequency of the oscillator can be estimated with the following equations: $$f_{OSC} = \frac{1.72}{R_{RT} \times C_{CT}} \quad (1)$$ where f_{OSC} is in Hertz, R_{RT} is in Ohms and C_{CT} is in Farads. Never use a timing resistor less than 5 kΩ. The frequency of the OUTPUT gate drive of the UCx842 and UCx843, f_{SW}, is equal to f_{OSC} at up to 100% duty cycle; the frequency of the UCx844 and UCx845 is equal to half of the f_{OSC} frequency at up to 50% duty cycle.
VC	—	11	17	I	Bias supply input for the output gate drive. For PWM controllers that do not have this pin, the gate driver is biased from the VCC pin. VC must have a bypass capacitor at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VCC	7	12	18	I	Analog controller bias input that provides power to the device. Total VCC current is the sum of the quiescent VCC current and the average OUTPUT current. Knowing the switching frequency and the MOSFET gate charge, Q_g, the average OUTPUT current can be calculated from: $$I_{OUTPUT} = Q_g \times f_{SW} \quad (2)$$ A bypass capacitor, typically 0.1 µF, connected directly to GROUND with minimal trace length, is required on this pin. An additional bypass capacitor at least 10 times greater than the gate capacitance of the main switching FET used in the design is also required on VCC.
VFB	2	3	5	I	Inverting input to the internal error amplifier. VFB is used to control the power converter voltage-feedback loop for stability.

Pin Functions (continued)

PIN				TYPE	DESCRIPTION
NAME	SOIC, CDIP, PDIP (8)	SOIC, CFP (14)	LCCC (20)		
VREF	8	14	20	O	5-V reference voltage. VREF is used to provide charging current to the oscillator timing capacitor through the timing resistor. It is important for reference stability that VREF is bypassed to GROUND with a ceramic capacitor connected as close to the pin as possible. A minimum value of 0.1-µF ceramic is required. Additional VREF bypassing is required for external loads on VREF.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VCC}	Low impedance source		30	V
	I_{VCC} < 30 mA	Self Limiting		
V_{VFB} and V_{ISENSE}	Analog input voltage	–0.3	6.3	V
V_{VC}	Input Voltage, Q and D Package only		30	V
I_{OUTPUT}	Output drive current		±1	A
I_{COMP}	Error amplifier output sink current		10	mA
E_{OUTPUT}	Output energy (capacitive load)		5	µJ
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±3000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{VCC} and V_{VC}(1)	Supply voltage		12		28	V
V_{VFB}	Input voltage				2.5	V
V_{ISENSE}	Input voltage				1	V
I_{VCC}	Supply current, externally limited				25	mA
I_{OUTPUT}	Average output current				200	mA
I_{VREF}	Reference output current				–20	mA
f_{OSC}	Oscillator frequency			100	500	kHz
T_A	Operating free-air temperature	UC184x	–55		125	°C
		UC284x	–40		85	
		UC384x	0		70	

(1) These recommended voltages for VC and POWER GROUND apply only to the D package.

7.4 Thermal Information

THERMAL METRIC(1)		UCx84x				UNIT
		D (SOIC)	D (SOIC)	P (PDIP)	FK (LCCC)	
		8 PINS	14 PINS	8 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.8	78.2	53.7	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.3	37.1	46.7	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	32.6	31	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	7.3	17.1	—	°C/W
ψ_{JB}	Junction-to-bottom characterization parameter	45.2	32.4	30.9	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		UCx84x				UNIT
		D (SOIC) 8 PINS	D (SOIC) 14 PINS	P (PDIP) 8 PINS	FK (LCCC) 20 PINS	
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	—	—	—	4.1	°C/W

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) –55°C ≤ T_A ≤ 125°C for the UC184x; –40°C ≤ T_A ≤ 85°C for the UC284x, 0°C ≤ T_A ≤ 70°C for the UC384x, V_{CC} = 15 V[1]; 0.1 µF capacitor from VCC to GROUND, 0.1 µF capacitor from VREF to GROUND, R_{RT} = 10 kΩ; C_{CT} = 3.3 nF, T_J = T_A.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE SECTION							
V_{VREF}	Reference voltage	I_{VREF} = 1 mA, T_J = 25°C	UC184x and UC284x	4.95	5	5.05	V
			UC384x	4.9	5	5.1	
	Line regulation	12 ≤ VCC ≤ 25 V			6	20	mV
	Load regulation	1 ≤ I_{VREF} ≤ 20 mA			6	25	mV
	Temperature stability	See [2] [3]			0.2	0.4	mV/°C
	Total output variation	Line, load, temperature [2]	UC184x and UC284x	4.9		5.1	V
			UC384x	4.82		5.18	
	Output noise voltage	10 Hz ≤ f_{OSC} ≤ 10 kHz, [2] T_J = 25°C			50		µV
	Long term stability	T_A = 125°C, 1000 Hrs [2]			5	25	mV
	Output short circuit			–30	–100	–180	mA
OSCILLATOR SECTION							
f_{OSC}	Initial accuracy	T_J = 25°C[4]		47	52	57	kHz
	Voltage stability	12 ≤ VCC ≤ 25 V			0.2%	1%	
	Temperature stability	T_{MIN} ≤ T_A ≤ T_{MAX} [2]			5%		
$V_{RT/CT}$	Amplitude	Peak-to-peak [2]			1.7		V
ERROR AMPLIFIER SECTION							
V_{VFB}	Input voltage	V_{COMP} = 2.5 V	UC184x and UC284x	2.45	2.5	2.55	V
			UC384x	2.42	2.5	2.58	
I_{VFB}	Input bias current		UC184x and UC284x			–1	µA
			UC384x			–2	
A_{VOL}		2 ≤ V_{COMP} ≤ 4 V		65	90		dB
	Unity gain bandwidth	T_J = 25°C [2]		0.7	1		MHz
PSRR	Power supply rejection ratio	12 ≤ VCC ≤ 25 V		60	70		dB
$I_{(snk)}$	COMP sink current	V_{VFB} = 2.7 V, V_{COMP} = 1.1 V		2	6		mA
$I_{(src)}$	COMP source current	V_{VFB} = 2.3 V, V_{COMP} = 5 V		–0.5	–0.8		

(1) Adjust VCC above the start threshold before setting at 15 V
(2) Specified by design. Not production tested.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{\text{VREF}_{(\max)} - \text{VREF}_{(\min)}}{T_{J(\max)} - T_{J(\min)}}$$

VREF_{min} and VREF_{max} are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) OUTPUT switching frequency, f_{SW}, equals the oscillator frequency, f_{OSC}, for the UCx842 and UCx843. OUTPUT switching frequency, f_{SW}, is one half oscillator frequency, f_{OSC}, for the UCx844 and UCx845.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) –55°C ≤ T_A ≤ 125°C for the UC184x; –40°C ≤ T_A ≤ 85°C for the UC284x, 0°C ≤ T_A ≤ 70°C for the UC384x, V_{VCC} = 15 V(1); 0.1 µF capacitor from VCC to GROUND, 0.1 µF capacitor from VREF to GROUND, R_{RT} = 10 kΩ; C_{CT} = 3.3 nF, T_J = T_A.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{COMP} High	High-level output voltage	V_{VFB} = 2.3 V, R_L = 15-kΩ COMP to GROUND	5	6		V
V_{COMP} Low	Low-level output voltage	V_{VFB} = 2.7 V, R_L = 15-kΩ COMP to VREF		0.7	1.1	V
CURRENT SENSE SECTION						
A_{CS}	Gain	See (5) (6)	2.85	3	3.15	V/V
V_{ISENSE}	Maximum input signal	V_{COMP} = 5 V (5)	0.9	1	1.1	V
PSRR	Power supply rejection ratio	12 V ≤ V_{VCC} ≤ 25 V (2) (5)		70		dB
I_{ISENSE}	Input bias current			–2	–10	µA
t_{DLY}	Delay to output	V_{ISENSE} stepped from 0 V to 2 V (2)		150	300	ns
OUTPUT SECTION						
V_{OUT} Low	Low-level OUTPUT voltage	I_{SINK} = 20 mA		0.1	0.4	V
		I_{SINK} = 200 mA		1.5	2.2	
V_{OUT} High	High-level OUTPUT voltage	I_{SOURCE} = 20 mA	13	13.5		V
		I_{SOURCE} = 200 mA	12	13.5		
t_{RISE}	Rise time (2)	C_{OUTPUT} = 1 nF, T_J = 25°C		50	150	ns
t_{FALL}	Fall time (2)	C_{OUTPUT} = 1 nF, T_J = 25°C,		50	150	ns
UNDERVOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	Enable threshold	UC1842/4 and UC2842/4	15	16	17	V
		UC3842/4	14.5	16	17.5	
		UCx843/5	7.8	8.4	9	
VCC_{OFF}	UVLO off threshold	UC1842/4 and UC2842/4	9	10	11	V
		UC3842/4	8.5	10	11.5	
		UCx843/5	7	7.6	8.2	
PWM						
D_{MAX}	Maximum duty cycle	UCx842/3	95%	97%	100%	
		UC1844/5 and UC2844/5	46%	48%	50%	
		UC3844/5	47%	48%	50%	
D_{MIN}	Minimum duty cycle				0%	
TOTAL STANDBY CURRENT						
I_{VCC}	Start-up current			0.5	1	mA
I_{VCC}	Operating supply current	V_{VFB} = V_{ISENSE}= 0 V		11	17	
	VCC Zener voltage	I_{VCC} = 25 mA	30	34		V

(5) Parameter measured at trip point of latch with VFB = 0 V.
(6) Gain defined as: A = $\Delta V_{COMP}/\Delta V_{ISENSE}$, 0 V ≤ V_{ISENSE} ≤ 0.8 V.

7.6 Typical Characteristics

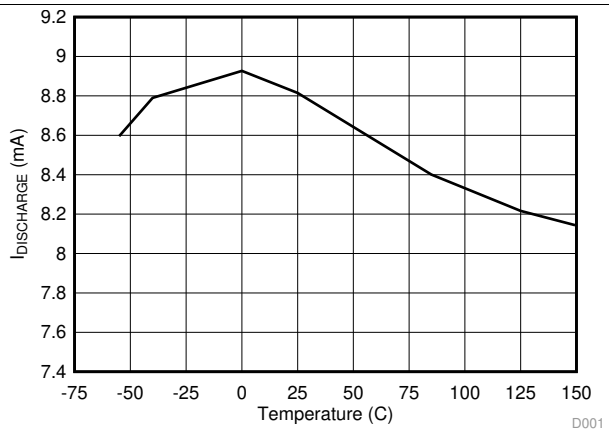


Figure 1. Oscillator Discharge Current vs Temperature for VCC = 15 V and V_{OSC} = 2 V

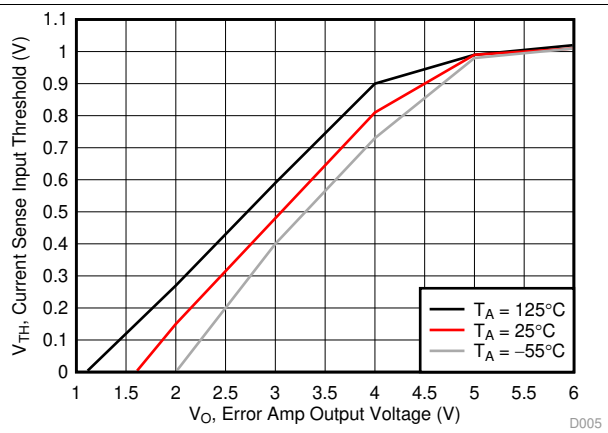


Figure 2. Current Sense Input Threshold vs Error Amplifier Output Voltage for VCC = 15 V

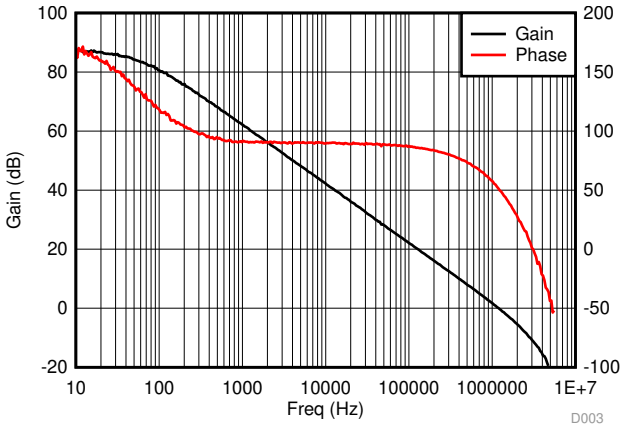


Figure 3. Error Amplifier Open-Loop Gain and Phase vs Frequency, VCC = 15 V, R_L = 100 kΩ, and T_A = 25 °C

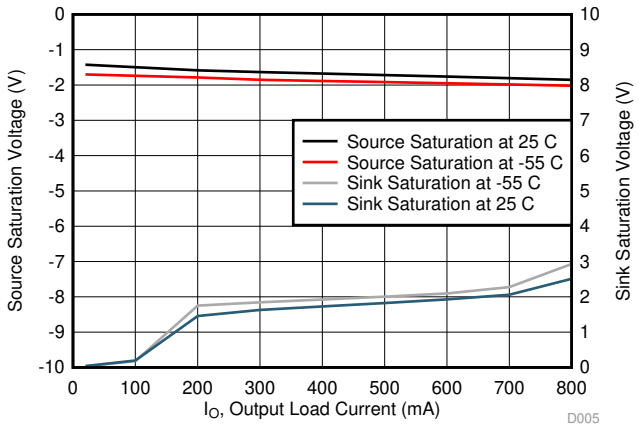


Figure 4. OUTPUT Saturation Voltage vs Load Current for VCC = 15 V with 5-ms Input Pulses

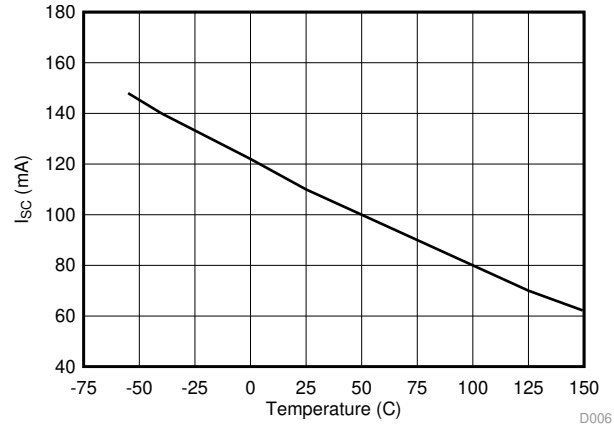


Figure 5. VREF Short-Circuit Current vs Temperature for VCC = 15 V

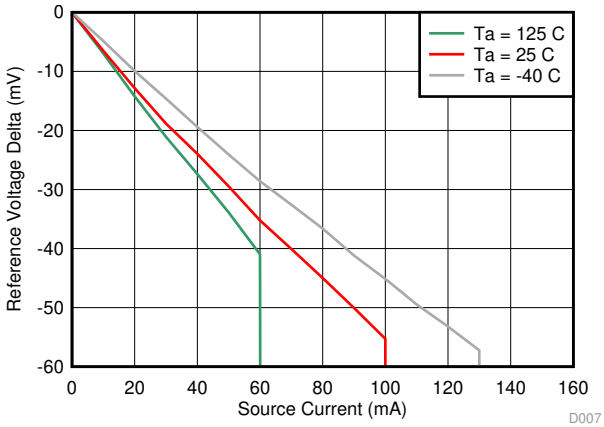


Figure 6. VREF Voltage vs Source Current

Typical Characteristics (continued)

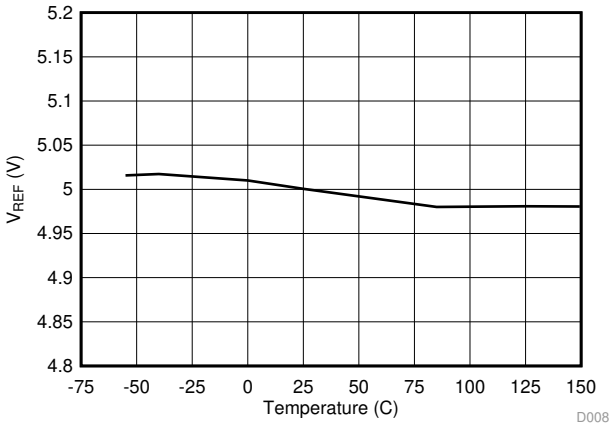


Figure 7. VREF Voltage vs Temperature

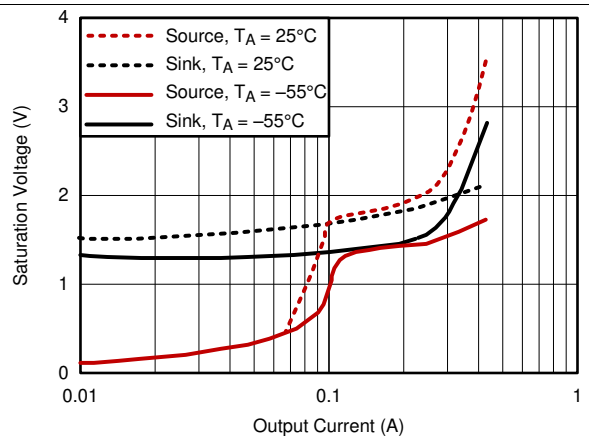


Figure 8. Output Saturation

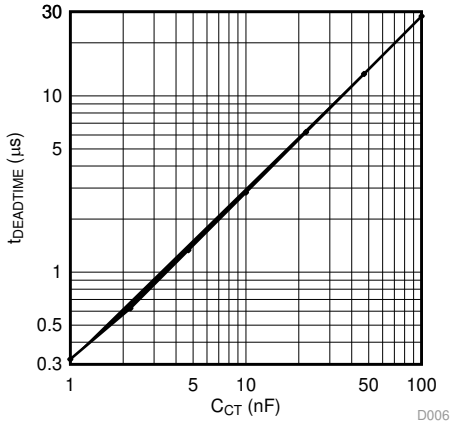


Figure 9. Dead Time vs Timing Capacitance, C_{CT}

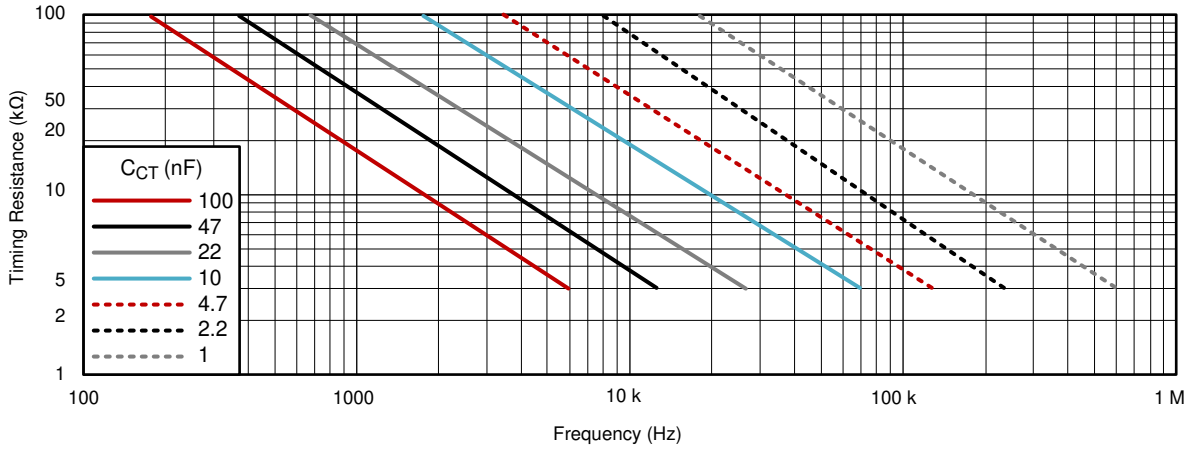


Figure 10. Timing Resistance, R_{RT}, vs Frequency

8 Detailed Description

8.1 Overview

The UCx84x series of control integrated circuits provide the features necessary to implement AC-DC or DC-to-DC fixed-frequency current-mode control schemes with a minimum number of external components. Protection circuitry includes undervoltage lockout (UVLO) and current limiting. Internally implemented circuits include a start-up current of less than 1 mA, a precision reference trimmed for accuracy at the error amplifier input, logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off-state.

Major differences between members of these series are the UVLO thresholds, acceptable ambient temperature range, and maximum duty-cycle. Typical UVLO thresholds of 16 V (ON) and 10 V (OFF) on the UCx842 and UCx844 devices make them ideally suited to off-line AC-DC applications. The corresponding typical thresholds for the UCx843 and UCx845 devices are 8.4 V (ON) and 7.6 V (OFF), making them ideal for use with regulated input voltages used in DC-DC applications. The UCx842 and UCx843 devices operate to duty cycles approaching 100%. The UCx844 and UCx845 obtain a duty-cycle range of 0% to 50% by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

The UC184x-series devices are characterized for operation from –55°C to 125°C. UC284x-series devices are characterized for operation from −40°C to 85°C. The UC384x devices are characterized for operation from 0°C to 70°C.

8.2 Functional Block Diagrams

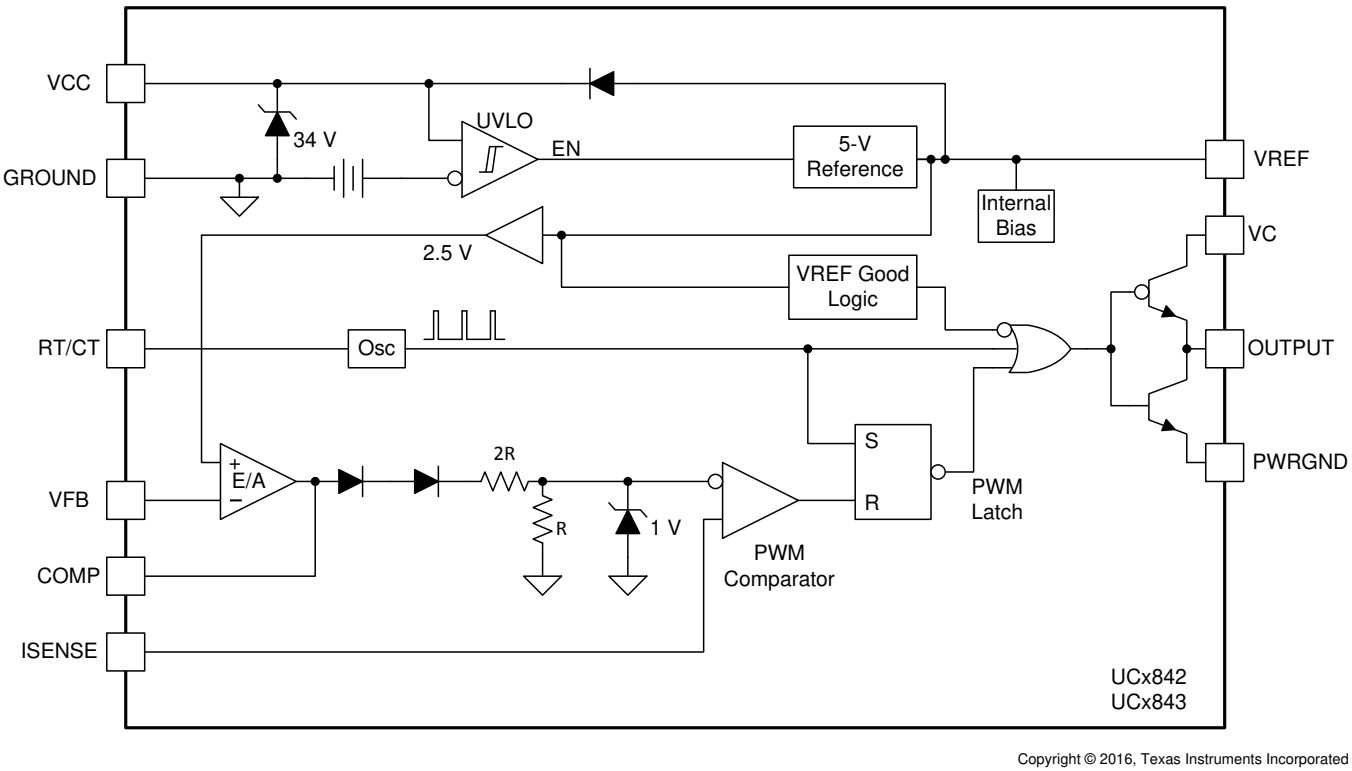


Figure 11. UCx842 and UCx843 Block Diagram, No Toggle

Functional Block Diagrams (continued)

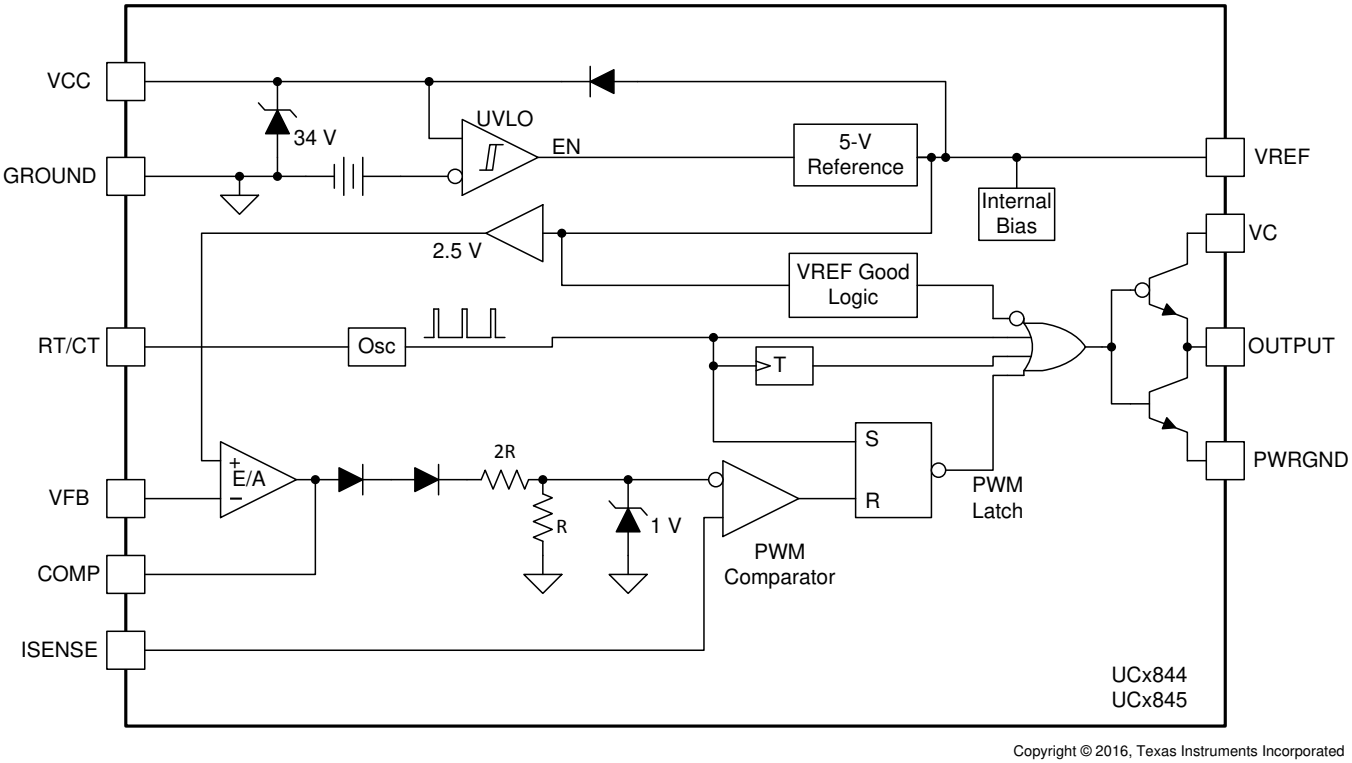


Figure 12. UCx844 and UCx845 Block Diagram, Toggle

8.3 Feature Description

8.3.1 Detailed Pin Description

8.3.1.1 COMP

The error amplifier in the UCx84x family is an open collector in parallel with a current source, with a unity-gain bandwidth of 1 MHz. The COMP terminal can both source and sink current. The error amplifier is internally current-limited, so that one can command zero duty cycle by externally forcing COMP to GROUND.

8.3.1.2 VFB

VFB is the inverting input of the error amplifier. VFB is used to control the power converter voltage-feedback loop for stability. For best stability, keep VFB lead length as short as possible and VFB stray capacitance as small as possible.

8.3.1.3 ISENSE

The UCx84x current sense input connects to the PWM comparator. Connect ISENSE to the MOSFET source current sense resistor. The PWM uses this signal to terminate the OUTPUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration or to add slope compensation. To prevent false triggering due to leading edge noises, an RC current sense filter may be required. The gain of the current sense amplifier is typically 3 V/V.

Feature Description (continued)

8.3.1.4 RT/CT

RT/CT is the oscillator timing pin. For fixed frequency operation, set the timing capacitor charging current by connecting a resistor from VREF to RT/CT. Set the frequency by connecting timing capacitor from RT/CT to GROUND. For the best performance, keep the timing capacitor lead to GROUND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The UCx84x's oscillator allows for operation to 500 kHz. The device uses an external resistor to set the charging current for the external capacitor, which determines the oscillator frequency. The recommended range of timing resistor values is between 5 kΩ and 100 kΩ; the recommended range of timing capacitor values is between 1 nF and 100 nF.

$$f_{OSC} = \frac{1.72}{R_{RT} \times C_{CT}} \quad (3)$$

In this equation, the switching frequency, f_{SW} is in Hz, R_{RT} is in Ω, and C_{CT} is in Farads.

8.3.1.5 GROUND

GROUND is the signal and power returning ground. TI recommends separating the signal return path and the high current gate driver path so that the signal is not affected by the switching current.

8.3.1.6 OUTPUT

The high-current bipolar totem-pole output of the UCx84x devices sinks or sources up to 1-A peak of current. The OUTPUT pin can directly drive a MOSFET. The OUTPUT of the UCx842 and UCx843 devices switches at the same frequency as the oscillator and can operate near 100% duty cycle. In the UCx844 and UCx845 devices, the switching frequency of OUTPUT is one-half that of the oscillator due to an internal T flipflop. This limits the maximum duty cycle in the UCx844 and UCx845 to < 50%. Schottky diodes may be necessary on the OUTPUT pin to prevent overshoot and undershoot due to high impedance to the supply rail and to ground, respectively. A bleeder resistor, placed between the gate and the source of the MOSFET, should be used to prevent activating the power switch with extraneous leakage currents during undervoltage lockout. An external clamp circuit may be necessary to prevent overvoltage stress on the MOSFET gate when VCC exceeds the gate voltage rating.

8.3.1.7 VCC

VCC is the power input connection for this device. In normal operation, power VCC through a current-limiting resistor. Although quiescent VCC current is only 0.5 mA, the total supply current is higher, depending on the OUTPUT current. Total VCC current is the sum of quiescent VCC current and the average OUTPUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUTPUT current can be calculated from Equation 4.

$$I_{OUTPUT} = Q_g \times f_{SW} \quad (4)$$

The UCx84x has a VCC supply voltage clamp of 34 V typical, but the absolute maximum value for VCC from a low-impedance source is 30 V. For applications that have a higher input voltage than the recommended VCC voltage, place a resistor in series with VCC to increase the source impedance. The maximum value of this resistor is calculated with Equation 5.

$$R_{VCC\,(max)} = \frac{V_{IN\,(min)} - V_{VCC\,(max)}}{I_{VCC} + \left(Q_g \times f_{SW}\right)} \quad (5)$$

In Equation 5, $V_{IN(min)}$ is the minimum voltage that is used to supply VCC, $V_{VCC(max)}$ is the maximum VCC clamp voltage and I_{VCC} is the IC supply current without considering the gate driver current and Q_g is the external power MOSFET gate charge and f_{SW} is the switching frequency.

The turnon and turnoff thresholds for the UCx84x family are significantly different: 16 V and 10 V for the UCx842 and UCx844; 8.4 V and 7.6 V for the UCx843 and UCx855. To ensure against noise related problems, filter VCC with an electrolytic and bypass with a ceramic capacitor to ground. Keep the capacitors close to the IC pins.

Feature Description (continued)

8.3.1.8 VREF

VREF is the voltage reference for the error amplifier and also for many other internal circuits in the IC. The high-speed switching logic uses VREF as the logic power supply. The 5-V reference tolerance is ±2% for the UCx84x family. The output short-circuit current is 30 mA. For reference stability and to prevent noise problems with high-speed switching transients, bypass VREF to ground with a ceramic capacitor close to the IC package. A minimum of 0.1-µF ceramic capacitor is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

When VCC is greater than 1 V and less than the UVLO threshold, a 5-kΩ resistor pulls VREF to ground. VREF can be used as a logic output indicating power-system status because when VCC is lower than the UVLO threshold, VREF is held low.

8.3.2 Pulse-by-Pulse Current Limiting

Pulse-by-pulse limiting is inherent in the current mode control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

8.3.3 Current-Sense

An external series resistor, R_{CS}, senses the current and converts this current into a voltage that becomes the input to the ISENSE pin. The ISENSE pin is the noninverting input to the PWM comparator. The ISENSE input is compared to a signal proportional to the error amplifier output voltage; the gain of the current sense amplifier is typically 3 V/V. The peak I_{SENSE} current is determined by Equation 6:

$$I_{SENSE} = \frac{V_{ISENSE}}{R_{CS}} \tag{6}$$

The typical value for V_{ISENSE} is 1 V. A small RC filter, R_{CSF} and C_{CSF}, may be required to suppress switch transients caused by the reverse recovery of a secondary side diode or equivalent capacitive loading in addition to parasitic circuit impedances. The time constant of this filter should be considerably less than the switching period of the converter.

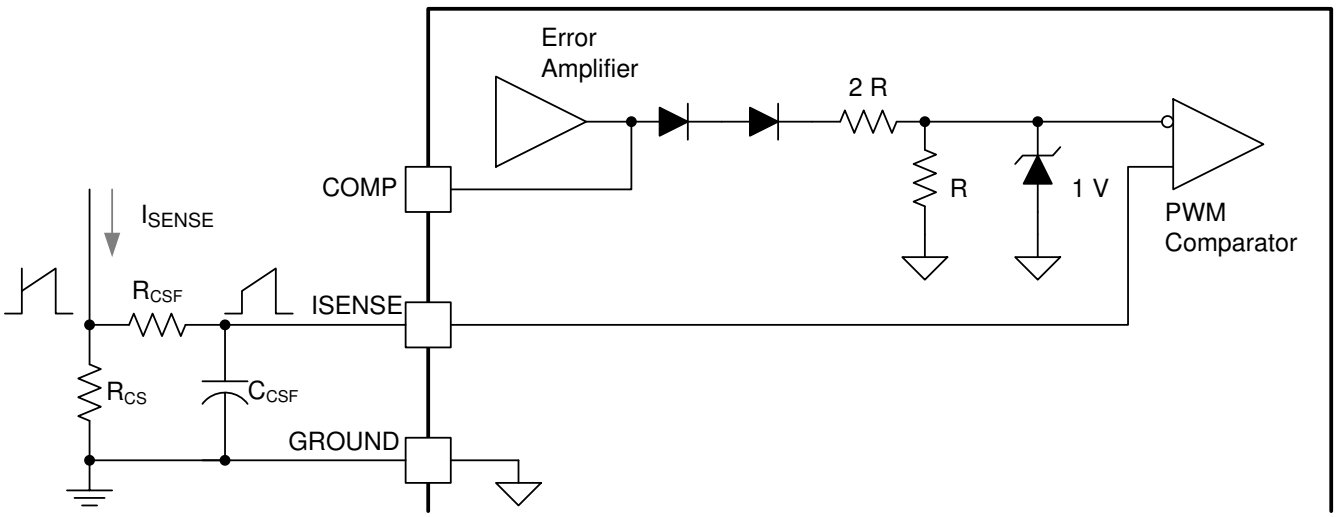


Figure 13. Current-Sense Circuit Schematic

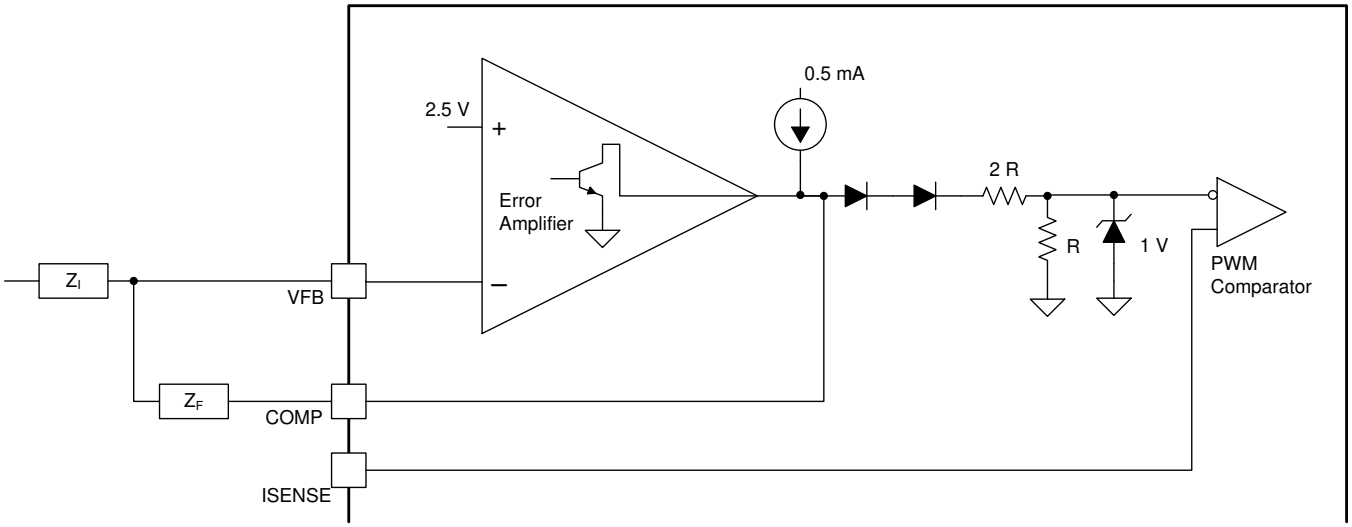
Feature Description (continued)

8.3.4 Error Amplifier With Low Output Resistance

The error amplifier output is an open collector in parallel with a current source. With a low output resistance, various impedance networks may be used on the compensation pin input for error amplifier feedback. The error amplifier output, COMP, is frequently used as a control port for secondary-side regulation by using an external secondary-side adjustable voltage regulator, such as a TL431, to send an error signal across the secondary-to-primary isolation boundary through an opto-isolator, in this configuration connect the COMP pin directly to the opto-isolator feedback. On the primary side, the inverting input to the UCx48x error amplifier, VFB, should be connected to GROUND. With VFB tied to GROUND, the error amplifier output, COMP, is forced to its high state and sources current, typically 0.8 mA. The opto-isolator must overcome the source current capability to control the COMP pin below the error amplifier output high level, VOH.

For primary-side regulation, configure the inverting input to the error amplifier, VFB, with a resistor divider to provide a signal that is proportional to the converter output voltage being regulated. Add the voltage loop compensation components between VFB and COMP. The internal noninverting input to the error amplifier is trimmed to 2.5 V. For best stability, keep VFB lead length as short as possible and minimize the stray capacitance on VFB.

The internal resistor divider on COMP is maintained at an R:2R ratio, the specific values of these internal resistors should not be critical in any application.



Error amplifier can source or sink up to 0.5 mA.

Figure 14. Error-Amplifier Configuration Schematic

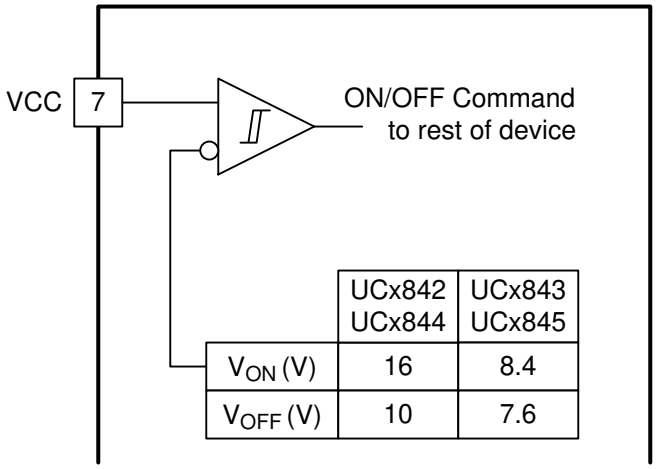
8.3.5 Undervoltage Lockout

The UCx84x devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. The UVLO circuit insures that VCC is adequate to make the UCx84x fully operational before enabling the output stage. Undervoltage lockout thresholds for the UCx842, UCx843, UCx844, and UCx845 devices are optimized for two groups of applications: off-line power supplies and DC-DC converters. The 6-V hysteresis in the UCx842 and UCx844 devices prevents VCC oscillations during power sequencing. This wider VCC_{ON} to VCC_{OFF} range, make these devices ideally suited to off-line AC input applications. The UCx843 and UCx845 controllers have a much narrower VCC_{ON} to VCC_{OFF} hysteresis and may be used in DC to DC applications where the input is considered regulated.

Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 17. During normal circuit operation, VCC is developed from auxiliary winding N_A with D_{BIAS} and C_{VCC}. At start-up, however, C_{VCC} must be charged to 16 V through R_{START}. With a start-up current of 1 mA, R_{START} can be as large as 100 kΩ and still charge C_{VCC} when V_{AC} = 90 V RMS (low line). Power dissipation in R_{START} would then be less than 350 mW even under high line (V_{AC}= 130 V RMS) conditions.

Feature Description (continued)

During UVLO the IC draws less than 1 mA of supply current. Once crossing the turnon threshold the IC supply current increases to a maximum of 17 mA, typically 11 mA, During undervoltage lockout, the output driver is biased to a high impedance state and sinks minor amounts of current. A bleeder resistor, placed between the gate and the source of the MOSFET should be used to prevent activating the power switch with extraneous leakage currents during undervoltage lockout.



	UCx842 UCx844	UCx843 UCx845
V_{ON} (V)	16	8.4
V_{OFF} (V)	10	7.6

Figure 15. UVLO Threshold

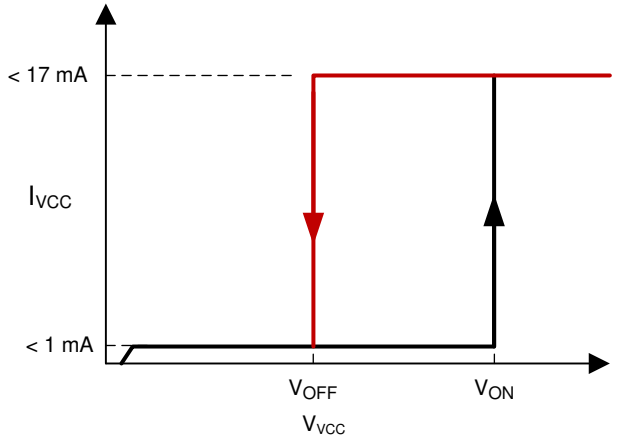


Figure 16. UVLO ON and OFF Profile

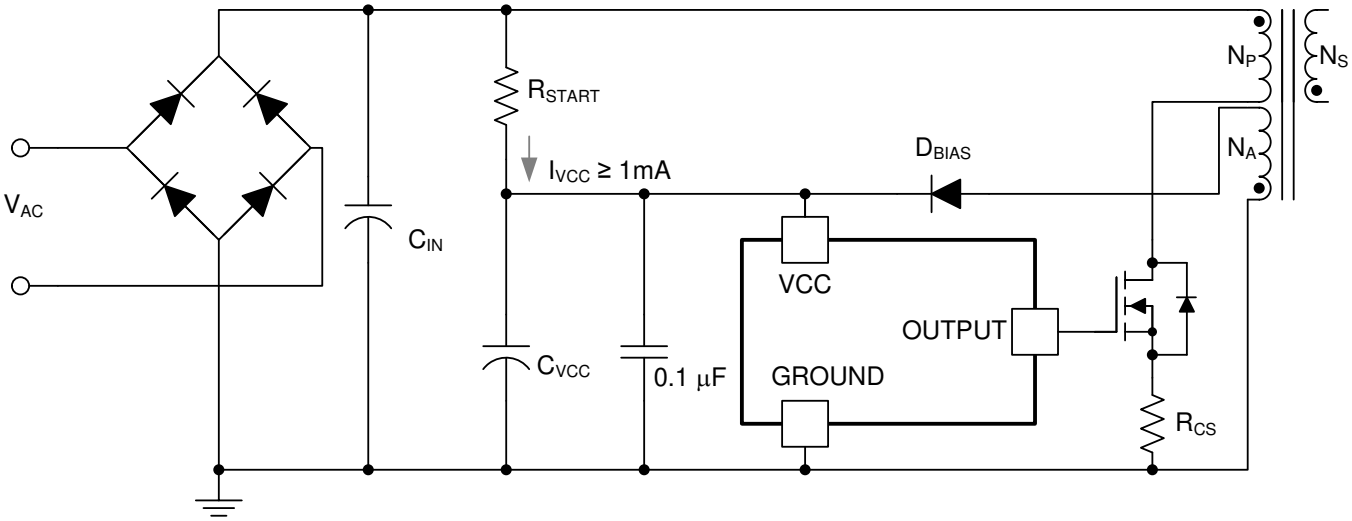


Figure 17. Providing Power to UCx84x

8.3.6 Oscillator

The oscillator allows for up to 500-kHz switching frequency. The OUTPUT gate drive is the same frequency as the oscillator in the UCx842 and UCx843 devices and can operate near 100% duty cycle. In the UCx844 and UCx845 devices, the frequency of OUTPUT is one-half that of the oscillator due to an internal T flipflop that blanks the output off every other clock cycle, resulting in a maximum duty cycle for these devices of < 50% of the switching frequency. An external resistor, R_{RT}, connected from VREF to RT/CT sets the charging current for the timing capacitor, C_{CT}, which is connected from RT/CT to GROUND. An R_{RT} value greater than 5 kΩ is recommended on RT/CT to set the positive ramp time of the internal oscillator. Using a value of 5 kΩ or greater for R_{RT} maintains a favorable ratio between the internal impedance and the external oscillator set resistor and results in minimal change in frequency over temperature. Using a value of less the recommended minimum value may result in frequency drift over temperature, part tolerances, or process variations.

Feature Description (continued)

The peak-to-peak amplitude of the oscillator waveform is 1.7 V in UCx84x devices. The UCx842 and UCx843 have a maximum duty cycle of approximately 100%, whereas the UCx844 and UCx845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the dead-time should not exceed 15% of the oscillator clock period. The discharge current, typically 6 mA at room temperature, sets the dead time, see Figure 9. During the discharge, or *dead* time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

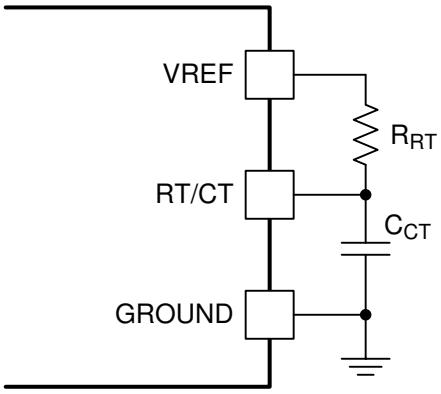
$$D_{MAX} = 1 - (t_{DEADTIME} \times f_{OSC}) \quad (7)$$

Equation 8 applies to UCx842 and UCx843 units because the OUTPUT switches at the same frequency as the oscillator and the maximum duty cycle can be as high as 100%.

$$D_{MAX} = 1 - \left(t_{DEADTIME} \times \frac{f_{OSC}}{2}\right) \quad (8)$$

Equation 8 applies to UCx844 and UCx845 units because the OUTPUT switches at half the frequency as the oscillator and the maximum duty cycle can be as high as 50%.

When the power transistor turns off, a noise spike is coupled to the oscillator RT/CT terminal. At high duty cycles, the voltage at RT/CT is approaching its threshold level (approximately 2.7 V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude prematurely trips the oscillator. To minimize the noise spike, choose C_{CT} as large as possible, remembering that dead time increases with C_{CT}. It is recommended that C_{CT} never be less than approximately 1000 pF. Often the noise which causes this problem is caused by the OUTPUT being pulled below ground at turnoff by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from GROUND to OUTPUT prevents such output noise from feeding to the oscillator.



For R_{RT} > 5 kΩ: $$f_{OSC} = \frac{1.72}{R_{RT} \times C_{CT}}$$

Figure 18. Oscillator Section Schematic

8.3.7 Synchronization

The simplest method to force synchronization uses the timing capacitor, C_{CT}, in near standard configuration. Rather than bring C_{CT} to ground directly, a small resistor is placed in series with C_{CT} to ground. This resistor serves as the input for the sync pulse which raises the C_{CT} voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_{RT} and C_{CT} until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator must be set to a lower frequency than the sync pulse stream, typically 20% with a 0.5-V pulse applied across the resistor.

Feature Description (continued)

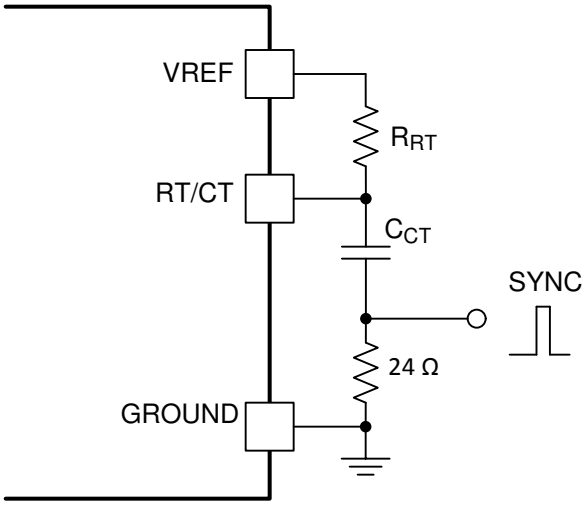


Figure 19. Synchronizing the Oscillator

8.3.8 Shutdown Technique

The PWM controller (see Figure 20) can be shut down by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (see *Figure 20*). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling VCC below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

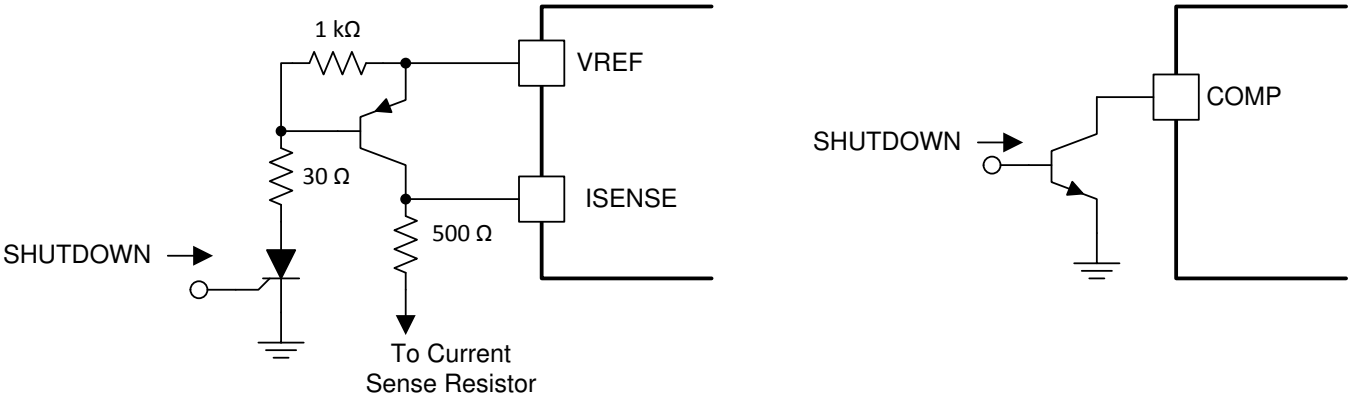


Figure 20. Shutdown Techniques

8.3.9 Slope Compensation

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 21). Note that capacitor C_{CSF} forms a filter with R_{CSF} to suppress the leading-edge switch spikes.

Feature Description (continued)

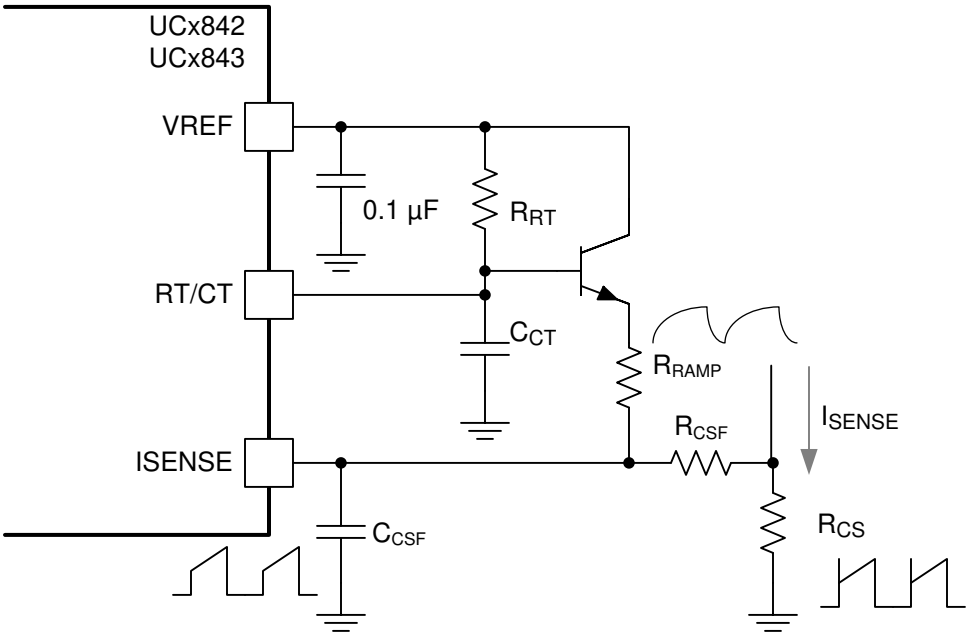


Figure 21. Slope Compensation

8.3.10 Soft Start

Upon power up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. The UCx84x devices do not have internal soft-start control, but this can be easily implemented externally with three components. An R/C network is used to provide the time constant to control the error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the RT/CT time constant by amplification through the transistors gain.

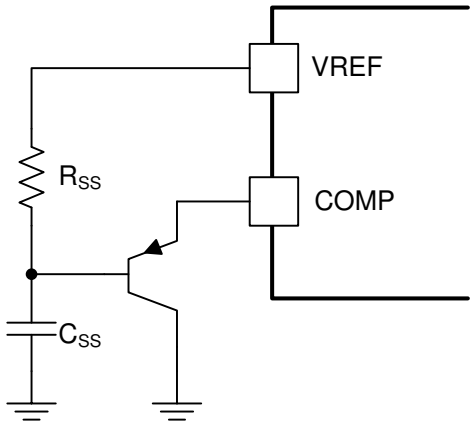


Figure 22. Soft-Start Circuitry

Feature Description (continued)

8.3.11 Voltage Mode

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor C_{CT} is used to generate a sawtooth waveform on both current or voltage mode ICs. To use the UCx84x in a voltage mode configuration, this sawtooth waveform will be input to the current sense input, ISENSE, for comparison to the error voltage at the PWM comparator. This sawtooth is used to determine pulse width instead of the actual primary current in this method. Loop compensation is similar to that of voltage mode controllers with subtle differences due to the low output resistance voltage amplifier in the UCx84x as opposed to a transconductance (current) type amplifier used in traditional voltage mode controllers. For further reference on topologies and compensation, consult *Closing the Feedback Loop* (SLUP068).

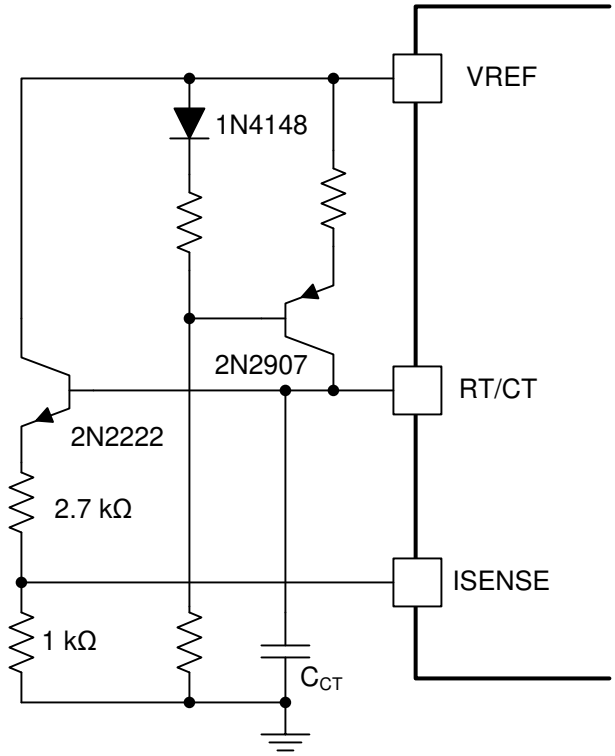


Figure 23. Current Mode PWM Used as a Voltage Mode PWM

8.4 Device Functional Modes

8.4.1 Normal Operation

During normal operating mode, the IC can be used in peak current mode or voltage mode control. When the converter is operating in peak current mode, the controller regulates the converter's peak current and duty cycle. When the IC is used in voltage mode control, the controller regulates the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

8.4.2 UVLO Mode

During the system start-up, VCC voltage starts to rise from 0 V. Before the VCC voltage reaches its corresponding turn on threshold, the IC is operating in UVLO mode. In this mode, the VREF pin voltage is not generated. When VCC is above 1 V and below the turnon threshold, the VREF pin is actively pulled low through a 5-kΩ resistor. This way, VREF can be used as a logic signal to indicate UVLO mode. If the bias voltage to VCC drops below the UVLO-off threshold, PWM switching stops and VREF returns to 0 V. The device can be restarted by applying a voltage greater than the UVLO-on threshold to the VCC pin.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCx84x controllers are peak current mode pulse width modulators. These controllers have an onboard amplifier and can be used in isolated and non-isolated power supply design. There is an onboard totem pole gate driver capable of delivering 1 A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 500 kHz.

9.1.1 Open-Loop Test Fixture

The following application is an open-loop laboratory test fixture. This circuit demonstrates the setup and use of the UCx84x devices and their internal circuitry.

In the open-loop laboratory test fixture (see Figure 24), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GROUND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

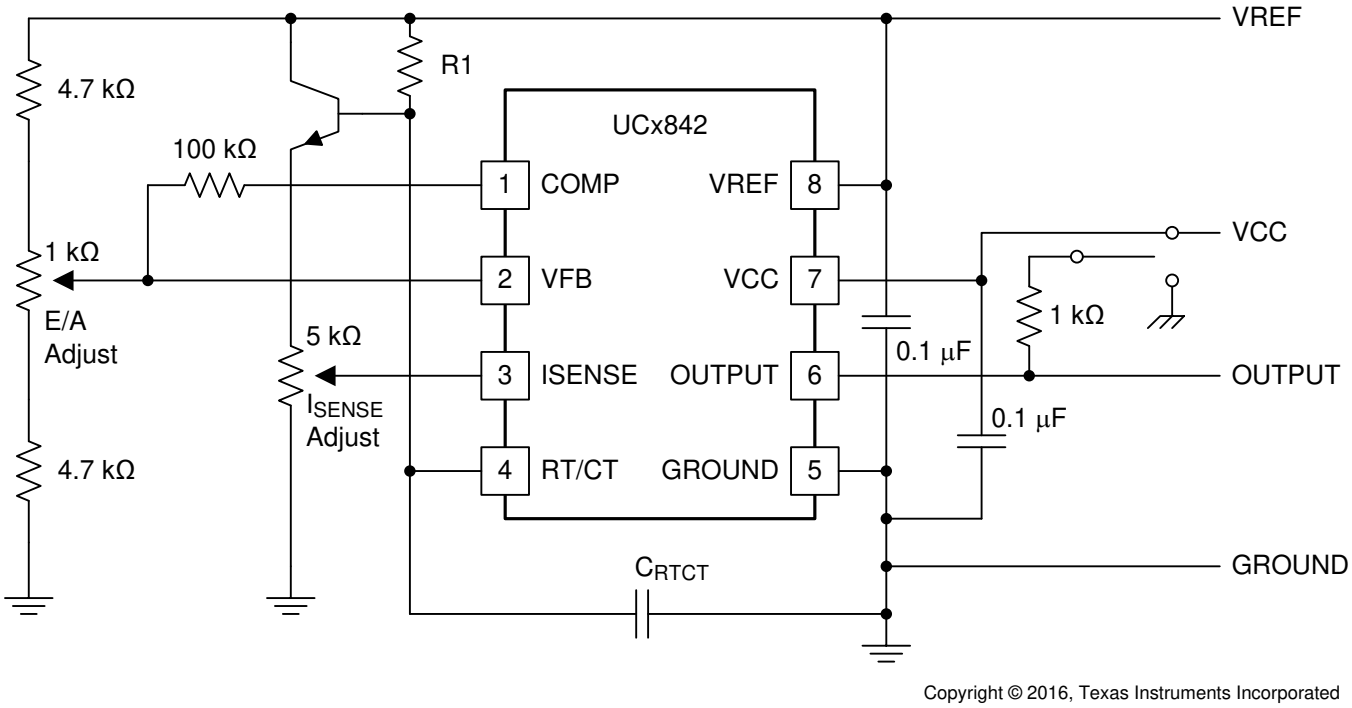


Figure 24. Open-Loop Laboratory Test Fixture

9.2 Typical Application

A typical application for the UC2842 in an off-line flyback converter is shown in Figure 25. The UC2842 uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage

Typical Application (continued)

at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to VFB. The outer voltage control loop determines the response to load changes.

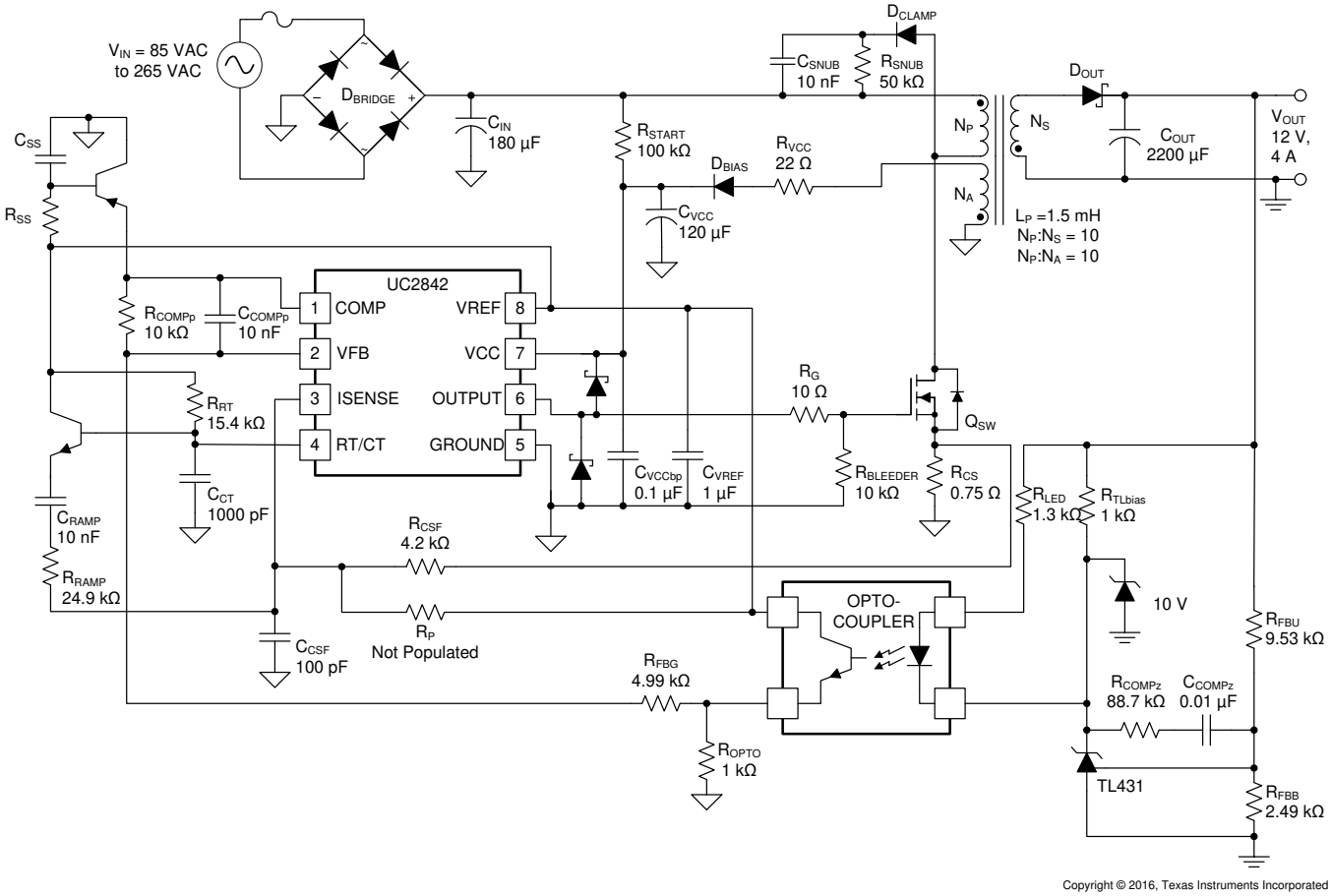


Figure 25. Typical Application Design Example Schematic

9.2.1 Design Requirements

Table 1 illustrates a typical set of performance requirements for an off-line flyback converter capable of providing 48 W at 12-V output voltage from a universal AC input. The design uses peak primary current control in a continuous current mode PWM converter.

Table 1. Performance Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage		85	115/230	265	V_{RMS}
f_{LINE}	Line Frequency		47	50/60	63	Hz
V_{OUT}	Output Voltage	$I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$	11.75	12	12.25	V
V_{RIPPLE}	Output Ripple Voltage	$I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$			100	mVpp
I_{OUT}	Output Current		0	4		A
f_{SW}	Switching Frequency			100		kHz
η	Efficiency			85%		

9.2.2 Detailed Design Procedure

This procedure outlines the steps to design an off-line universal input continuous current mode (CCM) flyback converter using the UC2842. See Figure 25 for component names referred to in the design procedure.

9.2.2.1 Input Bulk Capacitor and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel, often with some inductance between them to suppress differential-mode conducted noise. The value of the input capacitor sets the minimum bulk voltage; setting the bulk voltage lower by using minimal input capacitance results in higher peak primary currents leading to more stress on the MOSFET switch, the transformer, and the output capacitors. Setting the bulk voltage higher by using a larger input capacitor results in higher peak current from the input source and the capacitor itself will be physically larger. Compromising between size and component stresses determines the acceptable minimum input voltage. The total required value for the primary-side bulk capacitance, C_{IN}, is selected based upon the power level of the converter, P_{OUT}, the efficiency target, η, the minimum input voltage, $V_{IN(min)}$, and is chosen to maintain an acceptable minimum bulk voltage level, $V_{BULK(min)}$, using Equation 9.

$$C_{IN} = \frac{2 \times P_{IN} \times \left(0.25 + \frac{1}{\pi} \times \arcsin\left(\frac{V_{BULK\,(min)}}{\sqrt{2} \times V_{IN\,(min)}}\right)\right)}{\left(2 \times V_{IN\,(min)}^2 - V_{BULK\,(min)}^2\right) \times f_{LINE\,(min)}} \tag{9}$$

In this equation, $V_{IN(min)}$ is the RMS value of the minimum AC input voltage, 85 VRMS, whose minimum line frequency is denoted as $f_{LINE(min)}$, equal to 47 Hz. Based on the C_{IN} equation, to achieve a minimum bulk voltage of 75 V, assuming 85% converter efficiency, the bulk capacitor should be larger than 126 µF; 180 µF was chosen for the design, taking into consideration component tolerances and efficiency estimation.

9.2.2.2 Transformer Turns Ratio and Maximum Duty Cycle

The transformer design starts with selecting a suitable switching frequency for the given application. The UC2842 is capable of switching up to 500 kHz but considerations such as overall converter size, switching losses, core loss, system compatibility, and interference with communication frequency bands generally determine an optimum frequency that should be used. For this off-line converter, the switching frequency, f_{SW}, is selected to be 110 kHz as a compromise to minimize the transformer size and the EMI filter size, and still have acceptable losses.

The transformer primary to secondary turns ratio, N_{PS}, can be selected based on the desired MOSFET voltage rating and the secondary diode voltage rating. Because the maximum input voltage is 265 VRMS, the peak bulk input voltage can be calculated as shown in Equation 10.

$$V_{BULK\,(max)} = \sqrt{2} \times V_{IN\,(max)} \approx 375\ V \tag{10}$$

To minimize the cost of the system, a readily available 650-V MOSFET is selected. Derating the maximum voltage stress on the drain to 80% of its rated value and allowing for a leakage inductance voltage spike of up to 30% of the maximum bulk input voltage, the reflected output voltage should be less than 130 V as shown in Equation 11.

$$V_{REFLECTED} = 0.8 \times \left(V_{DS(rated)} - 1.3 \times V_{BULK(max)}\right) = 130.2\ V \tag{11}$$

The maximum primary to secondary transformer turns ratio, N_{PS}, for a 12 V output can be selected as

$$N_{PS} = \frac{V_{REFLECTED}}{V_{OUT}} = 10.85 \tag{12}$$

A turns ratio of N_{PS} = 10 is used in the design example.

The auxiliary winding is used to supply bias voltage to the UC2842. Maintaining the bias voltage above the VCC minimum operating voltage after turn on is required for stabile operation. The minimum VCC operating voltage for the UC2842 version of the controller is 10 V. The auxiliary winding is selected to support a 12-V bias voltage so that it is above the minimum operating level but still keeps the losses low in the IC. The primary to auxiliary turns ratio, N_{PA}, can be calculated from Equation 13:

$$N_{PA} = N_{PS} \times \frac{V_{OUT}}{V_{BIAS}} = 10 \tag{13}$$

The output diode experiences a voltage stress that is equal to the output voltage plus the reflected input voltage:

$$V_{DIODE} = \frac{V_{BULK\,(max)}}{N_{PS}} + V_{OUT} = 49.5\ V \tag{14}$$

To allow for voltage spikes due to ringing, a Schottky diode with a rated blocking voltage of greater than 60 V is recommended for this design. The forward voltage drop, V_F, of this diode is estimated to be equal to 0.6 V

To avoid high peak currents, the flyback converter in this design operates in continuous conduction mode. Once N_{PS} has been determined, the maximum duty cycle, D_{MAX}, can be calculated using the transfer function for a CCM flyback converter:

$$\frac{V_{OUT} + V_F}{V_{BULK\,(min)}} = \left(\frac{1}{N_{PS}}\right) \times \left(\frac{D_{MAX}}{1 - D_{MAX}}\right) \tag{15}$$

$$D_{MAX} = \frac{N_{PS} \times (V_{OUT} + V_F)}{V_{BULK(min)} + N_{PS} \times (V_{OUT} + V_F)} = 0.627 \tag{16}$$

Because the maximum duty cycle exceeds 50%, and the design is an off-line (AC-input) application, the UC2842 is best suited for this application.

9.2.2.3 Transformer Inductance and Peak Currents

For this design example, the transformer magnetizing inductance is selected based upon the CCM condition. An inductance value that allows the converter to stay in CCM over a wider operating range before transitioning into discontinuous current mode is used to minimize losses due to otherwise high currents and also to decrease the output ripple. The design of the transformer in this example sizes the inductance so the converter enters CCM operation at approximately 10% load and minimum bulk voltage to minimize output ripple.

The inductor, L_P for a CCM flyback can be calculated using Equation 17.

$$L_P = \frac{1}{2} \times \frac{(V_{BULK\,(min)})^2 \times \left(\frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + N_{PS} \times V_{OUT}}\right)^2}{0.1 \times P_{IN} \times f_{SW}} \tag{17}$$

In Equation 17, the input power, P_{IN}, is estimated by dividing the maximum output power, P_{OUT}, by the target efficiency, η, and f_{SW} is the switching frequency; for the UC2842 the switching frequency is equal to the oscillator frequency and is set to 110 kHz. Therefore, the transformer inductance should be approximately 1.8 mH; a 1.5-mH inductance is chosen as the magnetizing inductance value for this design.

Based on calculated inductor value and the switching frequency, the current stress of the MOSFET and output diode can be calculated.

The peak current in the primary-side MOSFET of a CCM flyback can be calculated as shown in Equation 18.

$$I_{PK_{MOSFET}} = \frac{P_{IN}}{V_{BULK\,(min)} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + (N_{PS} \times V_{OUT})}} + \left(\frac{V_{BULK\,(min)}}{2 \times L_m} \times \frac{\frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + (N_{PS} \times V_{OUT})}}{f_{SW}}\right) \tag{18}$$

The MOSFET peak current is 1.36 A. The RMS current of the MOSFET is calculated to be 0.97 A as shown in Equation 19. Therefore, IRFB9N65A is selected to be used as the primary-side switch.

$$I_{RMS_{MOSFET}} = \sqrt{\frac{D_{MAX}^3}{3} \times \left(\frac{V_{BULK\,(min)}}{L_P \times f_{SW}}\right)^2 - \left(\frac{D_{MAX}^2 \times I_{PK_{MOSFET}} \times V_{BULK\,(min)}}{L_P \times f_{SW}}\right) + \left(D_{MAX} \times I_{PK_{MOSFET}}^2\right)} \tag{19}$$

The output diode peak current is equal to the MOSFET peak current reflected to the secondary side.

$$I_{PK_{DIODE}} = N_{PS} \times I_{PK_{MOSFET}} = 13.634\ A \tag{20}$$

The diode average current is equal to the total output current, 4 A; combined with a required 60-V rating and 13.6-A peak current requirement, a 48CTQ060-1 is selected for the output diode.

9.2.2.4 Output Capacitor

The total output capacitance is selected based upon the output voltage ripple requirement. In this design, 0.1% voltage ripple is assumed. Based on the 0.1% ripple requirement, the capacitor value can be selected using Equation 21.

$$C_{OUT} \geq \frac{I_{OUT} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + N_{PS} \times V_{OUT}}}{0.001 \times V_{OUT} \times f_{SW}} = 1865\ \mu F \tag{21}$$

To design for device tolerances, a 2200-µF capacitor was selected.

9.2.2.5 Current Sensing Network

The current sensing network consists of the primary-side current sensing resistor, R_{CS}, filtering components R_{CSF} and C_{CSF}, and optional R_P. Typically, the direct current sense signal contains a large amplitude leading edge spike associated with the turnon of the main power MOSFET, reverse recovery of the output rectifier, and other factors including charging and discharging of parasitic capacitances. Therefore, C_{CSF} and R_{CSF} form a low-pass filter that provides immunity to suppress the leading edge spike. For this converter, C_{CSF} is chosen to be 100 pF.

Without R_P, R_{CS} sets the maximum peak current in the transformer primary based on the maximum amplitude of the ISENSE pin, which is specified to be 1 V. To achieve 1.36-A primary side peak current, a 0.75-Ω resistor is chosen for R_{CS}.

The high current sense threshold of ISENSE helps to provide better noise immunity to the system but also results in higher losses in the current sense resistor. These current sense losses can be minimized by injecting an offset voltage into the current sense signal using R_P. R_P and R_{CSF} form a resistor divider network from the current sense signal to the device's reference voltage, VREF, which adds an offset to the current sense voltage. This technique still achieves current mode control with cycle-by-cycle over-current protection. To calculate required offset value (V_{OFFSET}), use Equation 22.

$$V_{OFFSET} = \frac{R_{CSF}}{R_{CSF} + R_P} \times V_{REF} \tag{22}$$

Once R_P is added, adjust the current sense resistor, R_{CS}, accordingly.

9.2.2.6 Gate Drive Resistor

R_G is the gate driver resistor for the power switch, Q_{SW}. The selection of this resistor value must be done in conjunction with EMI compliance testing and efficiency testing. Using a larger resistor value for R_G slows down the turnon and turnoff of the MOSFET. A slower switching speed reduces EMI but also increases the switching loss. A trade-off between switching loss and EMI performance must be carefully performed. For this design, a 10-Ω resistor was chosen for the gate drive resistor.

9.2.2.7 VREF Capacitor

A precision 5-V reference voltage performs several important functions. The reference voltage is divided down internally to 2.5 V and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds. Therefore, the reference voltage must be bypassed with a ceramic capacitor (C_{VREF}), a 1-µF, 16-V ceramic capacitor was selected for this converter. Placement of this capacitor on the physical printed-circuit board layout must be as close as possible to the respective VREF and GROUND pins.

9.2.2.8 RT/CT

The internal oscillator uses a timing capacitor (C_{CT}) and a timing resistor (R_{RT}) to program the oscillator frequency and maximum duty cycle. The operating frequency can be programmed based the curves in *Application Curves*, where the timing resistor can be found once the timing capacitor is selected. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 15.4 kΩ and 1000 pF were selected for R_{RT} and C_{CT} to operate at 110-kHz switching.

9.2.2.9 Start-Up Circuit

At start-up, the IC gets its power directly from the high-voltage bulk, through a high-voltage resistor R_{START}. The selection of the start-up resistor is the trade-off between power loss and start-up time. The current flowing through R_{START} at the minimum input voltage must be higher than the VCC current under UVLO conditions (1 mA at its maximum value). A resistance of 100-kΩ was chosen for R_{START}, providing 1 mA of start-up current at low-line conditions. The start-up resistor is physically comprised of two 50-kΩ resistors in series to meet the high voltage requirements and power rating at high-line.

After VCC is charged up above the UVLO-on threshold, the UC2842 starts to consume full operating current. The VCC capacitor is required to provide enough energy to prevent its voltage from dropping below the UVLO-off threshold during start-up, before the output is able to reach its regulated level. A large bulk capacitance would hold more energy but would result in slower start-up time. In this design, a 120-µF capacitor is chosen to provide enough energy and maintain a start-up time of approximately 2 seconds.

9.2.2.10 Voltage Feedback Compensation

Feedback compensation, also called closed-loop control, can reduce or eliminate steady state error, reduce the sensitivity of the system to parametric changes, change the gain or phase of a system over some desired frequency range, reduce the effects of small signal load disturbances and noise on system performance, and create a stable system from an unstable system. A system is stable if its response to a perturbation is that the perturbation eventually dies out. A peak current mode flyback uses an outer voltage feedback loop to stabilize the converter. To adequately compensate the voltage loop, the open-loop parameters of the power stage must be determined.

9.2.2.10.1 Power Stage Poles and Zeroes

The first step in compensating a fixed frequency flyback is to verify if the converter is continuous conduction mode (CCM) or discontinuous conduction mode (DCM). If the primary inductance, L_P, is greater than the inductance for DCM/CCM boundary mode operation, called the critical inductance, or L_{Pcrit}, then the converter operates in CCM:

$$L_P > L_{Pcrit}\text{, then CCM} \tag{23}$$

$$L_{Pcrit} = \frac{R_{OUT} \times (N_{PS})^2}{2 \times f_{SW}} \times \left(\frac{V_{IN}}{V_{IN} + V_{OUT} \times N_{PS}}\right)^2 \tag{24}$$

For the entire input voltage range, the selected inductor has value larger than the critical inductor. Therefore, the converter operates in CCM and the compensation loop requires design based on CCM flyback equations.

The current-to-voltage conversion is done externally with the ground-referenced current sense resistor, R_{CS}, and the internal resistor divider of 2R/R which sets up the internal current sense gain, A_{CS} = 3. Note that the exact value of these internal resistors is not critical but the IC provides tight control of the resistor divider ratio, so regardless of the actual resistor value variations their relative value to each other is maintained.

The DC open-loop gain, G_O, of the fixed-frequency voltage control loop of a peak current mode control CCM flyback converter shown in Equation 25 is approximated by first using the output load, R_{OUT}, the primary to secondary turns ratio, N_{PS}, the maximum duty cycle, D, calculated in Equation 25.

$$G_O = \frac{R_{OUT} \times N_{PS}}{R_{CS} \times A_{CS}} \times \frac{1}{\frac{(1-D)^2}{\tau_L} + (2 \times M) + 1} \tag{25}$$

In Equation 25, D is calculated with Equation 26, τ_L is calculated with Equation 27, and M is calculated with Equation 28.

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULKmin} + (N_{PS} \times V_{OUT})} \tag{26}$$

$$\tau_L = \frac{2 \times L_P \times f_{SW}}{R_{OUT} \times (N_{PS})^2} \tag{27}$$

$$M = \frac{V_{OUT} \times N_{PS}}{V_{BULKmin}} \tag{28}$$

For this design, a converter with an output voltage V_{OUT} of 12 V, and 48 W relates to an output load, R_{OUT}, equal to 3 Ω at full load. With a maximum duty cycle calculated to be 0.627, a current sense resistance, R_{CS}, of 0.75 Ω, and a primary to secondary turns-ratio, N_{PS}, of 10, the open-loop gain calculates to 3.082, or 9.776 dB.

A CCM flyback has two zeroes that are of interest. The ESR and the output capacitance contribute a left-half plane zero, ω_{ESRz}, to the power stage, and the frequency of this zero, f_{ESRz}, are calculated with Equation 30.

$$\omega_{ESRz} = \frac{1}{R_{ESR} \times C_{OUT}} \quad (29)$$

$$f_{ESRz} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \quad (30)$$

The f_{ESRz} zero for an output capacitance of 2200 µF and a total ESR of 43 mΩ is located at 1.682 kHz.

CCM flyback converters have a zero in the right-half plane, RHP, in their transfer function. A RHP zero has the same 20 dB/decade rising gain magnitude with increasing frequency just like a left-half plane zero, but it adds a 90° phase lag instead of lead. This phase lag tends to limit the overall loop bandwidth. The frequency location, f_{RHPz}, of the RHP zero, ω_{RHPz}, is a function of the output load, the duty cycle, the primary inductance, L_P, and the primary to secondary side turns ratio, N_{PS}.

$$\omega_{RHPz} = \frac{R_{OUT} \times (1 - D)^2 \times (N_{PS})^2}{L_P \times D} \quad (31)$$

$$f_{RHPz} = \frac{R_{OUT} \times (1 - D)^2 \times (N_{PS})^2}{2 \times \pi \times L_P \times D} \quad (32)$$

The right-half plane zero frequency increases with higher input voltage and lighter load. Generally, the design requires consideration of the worst case of the lowest right-half plane zero frequency and the converter must be compensated at the minimum input and maximum load condition. With a primary inductance of 1.5 mH, at 75-V DC input, the RHP zero frequency, f_{RHPz}, is equal to 7.07 kHz at maximum duty cycle, full load.

The power stage has one dominate pole, ω_{P1}, which is in the region of interest, located at a lower frequency, f_{P1}, which is related to the duty cycle, D, the output load, and the output capacitance, calculated with Equation 34. There is also a double pole placed at half the switching frequency of the converter, f_{P2} calculated with Equation 36. For this example, pole f_{P1} is located at 40.37 Hz and f_{P2} is at 55 kHz.

$$\omega_{P1} = \frac{\frac{(1 - D)^3}{\tau_L} + 1 + D}{R_{OUT} \times C_{OUT}} \quad (33)$$

$$f_{P1} = \frac{\frac{(1 - D)^3}{\tau_L} + 1 + D}{2 \times \pi \times R_{OUT} \times C_{OUT}} \quad (34)$$

$$\omega_{P2} = \pi \times f_{SW} \quad (35)$$

$$f_{P2} = \frac{f_{SW}}{2} \quad (36)$$

9.2.2.10.2 Slope Compensation

Slope compensation is the large signal sub-harmonic instability that can occur with duty cycles that may extend beyond 50% where the rising primary side inductor current slope may not match the falling secondary side current slope. The sub-harmonic oscillation would result in an increase in the output voltage ripple and may even limit the power handling capability of the converter.

The target of slope compensation is to achieve an ideal quality coefficient, Q_P , to be equal to 1 at half of the switching frequency. The Q_P is calculated with Equation 37.

$$Q_P = \frac{1}{\pi \times [M_C \times (1 - D) - 0.5]} \quad (37)$$

In Equation 37, D is the primary side switch duty cycle and M_C is the slope compensation factor, which is defined with Equation 38.

$$M_C = \frac{S_e}{S_n} + 1 \tag{38}$$

In Equation 38, S_e is the compensation ramp slope and the S_n is the inductor rising slope. The optimal goal of the slope compensation is to achieve Q_P equal to 1; upon rearranging Equation 38 the ideal value of slope compensation factor is determined:

$$M_{ideal} = \frac{\frac{1}{\pi} + 0.5}{1 - D} \tag{39}$$

For this design to have adequate slope compensation, M_C must be 2.193 when D reaches it maximum value of 0.627.

The inductor rising slope, S_n, at the ISENSE pin is calculated with Equation 40.

$$S_n = \frac{V_{INmin} \times R_{CS}}{L_P} = 0.038 \ \frac{V}{\mu s} \tag{40}$$

The compensation slope, S_e, is calculated with Equation 41.

$$S_e = (M_C - 1) \times S_n = 44.74 \ \frac{mV}{\mu s} \tag{41}$$

The compensation slope is added into the system through R_{RAMP} and R_{CSF}. The C_{RAMP} is an AC-coupling capacitor that allows the voltage ramp of the oscillator to be used without adding an offset to the current sense; select a value to approximate high frequency short circuit, such as 10 nF as a starting point and make adjustments if required. The R_{RAMP} and R_{CSF} resistors form a voltage divider from the oscillator charge slope and this proportional ramp is injected into the ISENSE pin to add slope compensation. Choose the value of R_{RAMP} to be much larger than the R_{RT} resistor so that it does not load down the internal oscillator and result in a frequency shift. The oscillator charge slope is calculated using the peak-to-peak voltage of the RT/CT sawtooth waveform, V_{OSCpp}, equal to 1.7 V, and the minimum on-time, as shown in Equation 43.

$$t_{ONmin} = \frac{D}{f_{SW}} \tag{42}$$

$$S_{OSC} = \frac{V_{OSCpp}}{t_{ONmin}} = \frac{1.7 \text{ V}}{5.7 \ \mu s} = 298 \ \frac{mV}{\mu s} \tag{43}$$

To achieve a 44.74-mV/µs compensation slope, R_{CSF} resistor is calculated with Equation 44. In this design, R_{RAMP} is selected as 24.9 kΩ, a 4.2-kΩ resistor was selected for R_{CSF}.

$$R_{CSF} = \frac{R_{RAMP}}{\frac{S_{OSC}}{S_e} - 1} \tag{44}$$

9.2.2.10.3 Open-Loop Gain

Once the power stage poles and zeros are calculated and the slope compensation is determined, the power stage open-loop gain and phase of the CCM flyback converter can be plotted as a function of frequency. The power stage transfer function can be characterized with Equation 45.

$$H_{OPEN}(s) = G_0 \times \frac{\left(1 + \frac{s(f)}{\omega_{ESRz}}\right) \times \left(1 - \frac{s(f)}{\omega_{RHPz}}\right)}{1 + \frac{s(f)}{\omega_{P1}}} \times \frac{1}{1 + \frac{s(f)}{\omega_{P2} \times Q_P} + \frac{s(f)^2}{(\omega_{P2})^2}} \tag{45}$$

The bode for the open-loop gain and phase can be plotted by using Equation 46.

$$Gain_{OPEN}(s) = 20 \times \log(|H_{OPEN}(s)|) \tag{46}$$

(see Figure 26 and Figure 27).

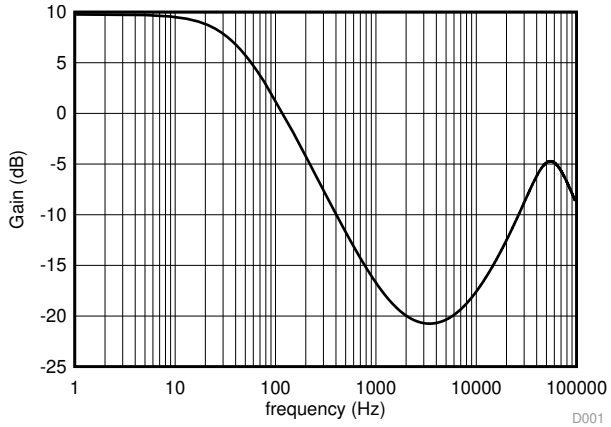


Figure 26. Converter Open-Loop Bode Plot - Gain

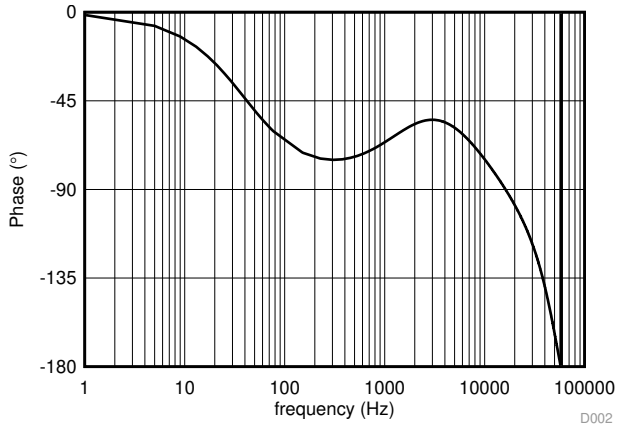


Figure 27. Converter Open-Loop Bode Plot - Phase

9.2.2.10.4 Compensation Loop

The design of the compensation loop involves selecting the appropriate components so that the required gain, poles, and zeros can be designed to result in a stabile system over the entire operating range. There are three distinct portions of the loop: the TL431, the opto-coupler, and the error amplifier. Each of these stages is combined with the power stage to result in a stable robust system.

For good transient response, the bandwidth of the finalized design should be as large as possible. The bandwidth of a CCM flyback, f_{BW}, is limited to ¼ of the RHP zero frequency, or approximately 1.77 kHz using Equation 47.

$$f_{BW} = \frac{f_{RHPz}}{4} \tag{47}$$

The gain of the open-loop power stage at f_{BW} can be calculated using Equation 46 or can be observed on the Bode plot (Figure 26) and is equal to –19.55 dB and the phase at f_{BW} is equal to –58°.

The secondary side portion of the compensation loop begins with establishing the regulated steady state output voltage. To set the regulated output voltage, a TL431 adjustable precision shunt regulator is ideally suited for use on the secondary side of isolated converters due to its accurate voltage reference and internal op amp. The resistors used in the divider from the output terminals of the converter to the TL431 REF pin are selected based upon the desired power consumption. Because the REF input current for the TL431 is only 2 µA, selecting the resistors for a divider current, I_{FB_REF}, of 1 mA results in minimal error. The top divider resistor, R_{FBU}, is calculated using Equation 48:

$$R_{FBU} = \frac{V_{OUT} - REF_{TL431}}{I_{FB\_REF}} \tag{48}$$

The TL431 reference voltage, REF_{TL431}, has a typical value of 2.495 V. A 9.53-kΩ resistor is chosen for R_{FBU}. To set the output voltage to 12 V, 2.49 kΩ is used for R_{FBB}.

$$R_{FBB} = \frac{REF_{TL431}}{V_{OUT} - REF_{TL431}} \times R_{FBU} \tag{49}$$

For good phase margin, a compensator zero, f_{COMPz}, is needed and should be placed at 1/10th the desired bandwidth:

$$f_{COMPz} = \frac{f_{BW}}{10} \tag{50}$$

$$\omega_{COMPz} = 2 \times \pi \times f_{COMPz} \tag{51}$$

With this converter, f_{COMPz} should be set at approximately 177 Hz. A series resistor, R_{COMPz}, and capacitor, C_{COMPz}, placed across the TL431 cathode to REF sets the compensator zero location. Setting C_{COMPz} to 0.01 µF, R_{COMPz} is calculated using Equation 52:

$$R_{COMPz} = \frac{1}{\omega_{COMPz} \times C_{COMPz}} \quad (52)$$

Using a standard value of 88.7 kΩ for R_Z and a 0.01 µF for C_Z results in a zero placed at 179 Hz.

Referring to Figure 25, R_{TLbias} provides cathode current to the TL431 from the regulated voltage provided from the Zener diode, D_{REG}. For robust performance, 10 mA is provided to bias the TL431 by way of the 10-V Zener and 1-kΩ resistor is used for R_{TLbias}.

The gain of the TL431 portion of the compensation loop can be written as:

$$G_{TL431}(s) = \left(R_{COMPz} + \frac{1}{s(f) \times C_{ZCOMPz}}\right) \times \frac{1}{R_{FBU}} \quad (53)$$

A compensation pole is needed at the frequency of right half plane zero or the ESR zero, whichever is lowest. Based previous the analysis, the right half plane zero, f_{RHPz}, is located at 7.07 kHz and the ESR zero, f_{ESRz}, is at 1.68 kHz; therefore, for this design, the compensation pole must be put at 1.68 kHz. The opto-coupler contains a parasitic pole that is difficult to characterize over frequency so the opto-coupler is set up with a pulldown resistor, R_{OPTO} equal to 1 kΩ, which moves the parasitic opto-coupler pole further out and beyond the range of interest for this design.

The required compensation pole can be added to the primary side error amplifier using R_{COMPp} and C_{COMPp}. Choosing R_{COMPp} as 10 kΩ, the required value of C_{COMPp} is determined using Equation 54.

$$C_{COMPp} = \frac{1}{2 \times \pi \times f_{ESRz} \times R_{COMPp}} = 9.46\ nF \quad (54)$$

A 10-nF capacitor is used for C_{COMPp} setting the compensation pole at 1.59 kHz.

Adding a DC gain to the primary side error amplifier may be required to obtain the required bandwidth and helps to adjust the loop gain as needed. Using a 4.99 kΩ for R_{FBG} sets the DC gain on the error amplifier to 2. At this point the gain transfer function of the error amplifier stage, $G_{EA}(s)$, of the compensation loop can be characterized:

$$G_{EA}(s) = \left(\frac{R_{COMPp}}{R_{FBG}}\right) \times \left(\frac{1}{1 + s(f) \times C_{COMPp} \times R_{COMPp}}\right) \quad (55)$$

Using an opto-coupler whose current transfer ratio (CTR) is typically at 100% in the frequency range of interest so that CTR = 1, the transfer function of the opto-coupler stage, $G_{OPTO}(s)$, is equal to:

$$G_{OPTO}(s) = \frac{CTR \times R_{OPTO}}{R_{LED}} \quad (56)$$

The bias resistor, R_{LED}, to the internal diode of the opto-coupler, and the pulldown resistor on the opto emitter, R_{OPTO}, sets the gain across the isolation boundary. R_{OPTO} has already been set to 1 kΩ but the value of R_{LED} has not yet been determined.

The total closed-loop gain, $G_{TOTAL}(s)$, is the combination of the open-loop power stage, $H_o(s)$, the opto gain, $G_{OPTO}(s)$, the error amplifier gain, $G_{EA}(s)$, and the gain of the TL431 stage, $G_{TL431}(s)$:

$$G_{TOTAL}(s) = |H_{OPEN}(s)| \times |G_{OPTO}(s)| \times |G_{EA}(s)| \times |G_{TL431}(s)| \quad (57)$$

The required value for R_{LED} can be selected to achieve the desired crossover frequency, f_{BW}. By setting the total loop gain equal to 1 at the desired crossover frequency and rearranging Equation 57, the optimal value for R_{LED} can be determined, as shown in Equation 58.

$$R_{LED} \leq |H_{OPEN}(s)| \times |CTR \times C_{OPTO}| \times |G_{EA}(s)| \times |G_{TL431}(s)| \quad (58)$$

A 1.3-kΩ resistor suits the requirement for R_{LED}.

Based on the compensation loop structure, the entire compensation loop transfer function is written as Equation 59.

$$G_{CLOSED}(s) = H_{OPEN}(s) \times \left(\frac{CTR \times R_{OPTO}}{R_{LED}}\right) \times \left(\frac{R_{COMPp}}{R_{FBG}}\right) \times \left(\frac{1}{1 + \left(s \times C_{COMPp} \times R_{COMPp}\right)}\right) \times \left(\frac{R_{COMPz} + \left(\frac{1}{s \times C_{COMPz}}\right)}{R_{FBU}}\right) \quad (59)$$

The final closed-loop bode plots are show in Figure 28 and Figure 29. The converter achieves a crossover frequency of approximately 1.8 kHz and has a phase margin of approximately 67°.

TI recommends checking the loop stability across all the corner cases including component tolerances to ensure system stability.

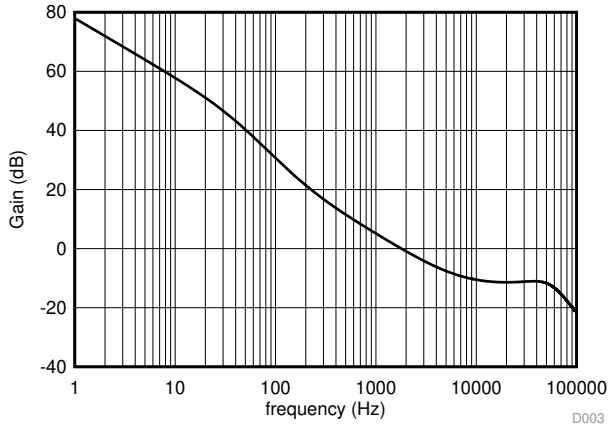


Figure 28. Converter Closed-Loop Bode Plot – Gain

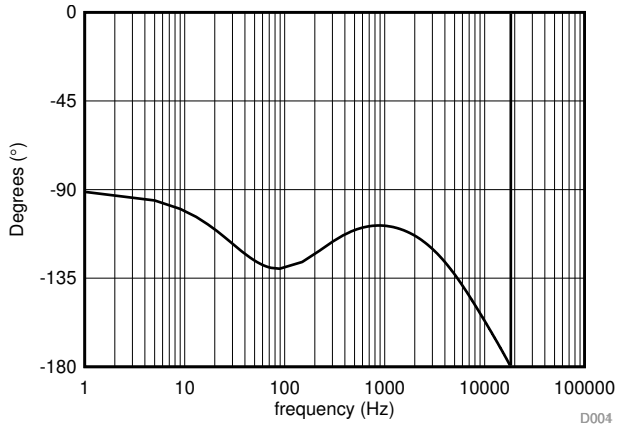


Figure 29. Converter Closed-Loop Bode Plot – Phase

9.2.3 Application Curves

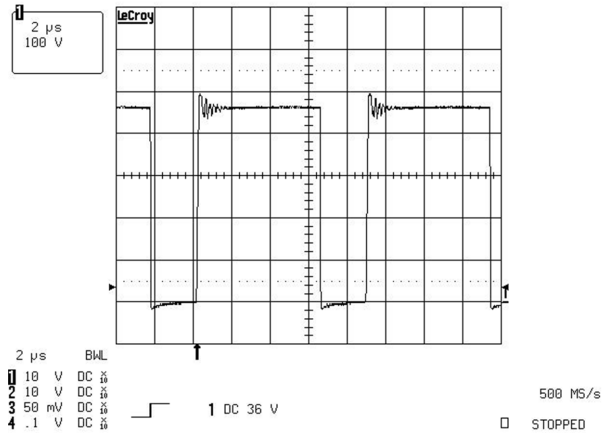


Figure 30. Primary Side MOSFET Drain to Source Voltage at 240-V AC Input (100 V/div)

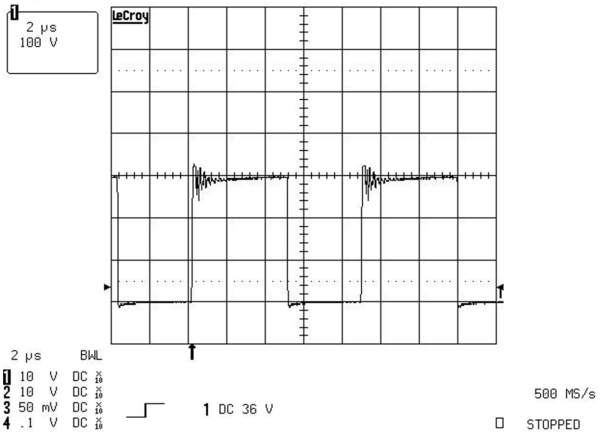


Figure 31. Primary Side MOSFET Drain to Source Voltage at 120-V AC Input (100 V/div)

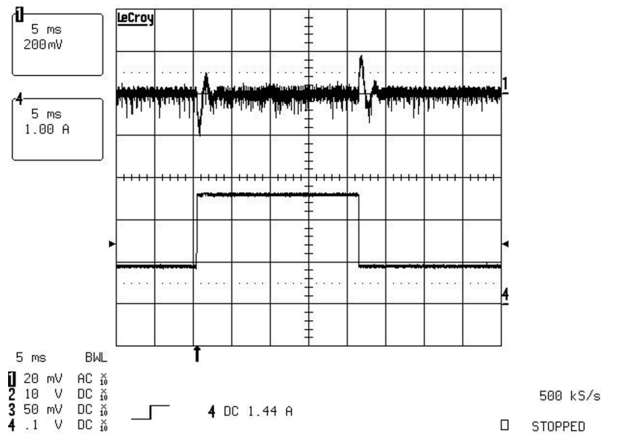


Figure 32. Output Voltage During 0.9-A to 2.7-A Load Transient (CH1: Output Voltage AC Coupled, 200 mV/div; CH4: Output Current, 1 A/div)

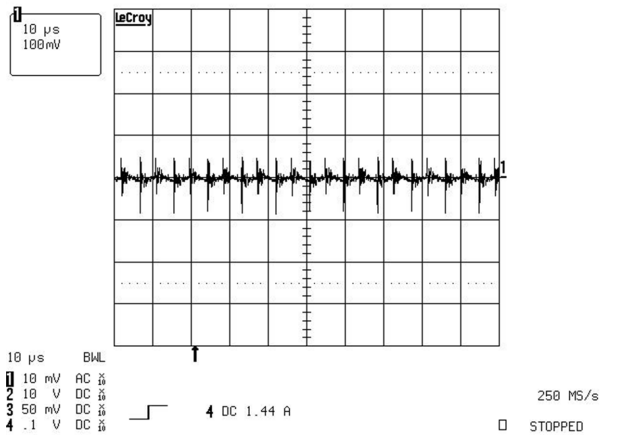


Figure 33. Output Voltage Ripple at Full Load (100 mV/div)

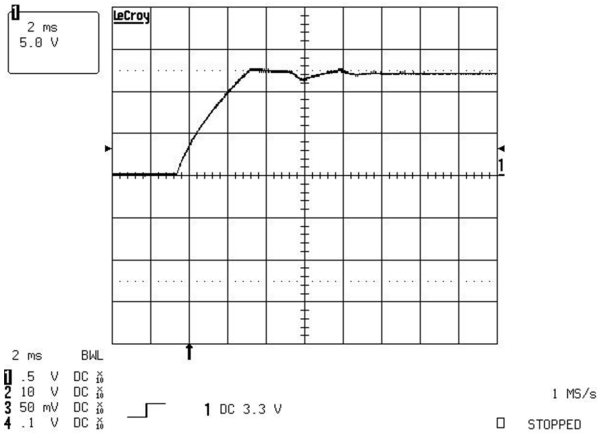


Figure 34. Output Voltage Behavior at Full Load Start-Up (5 V/div)

10 Power Supply Recommendations

It is important to bypass the ICs supply (VCC) and reference voltage (VREF) pins with a 0.1-µF to 1-µF ceramic capacitor to ground. The capacitors must be placed as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in offline applications to hold the supply voltage (VCC) above the UVLO turnoff threshold during start-up.

To prevent false triggering due to leading edge noises, an RC current sense filter may be required on ISENSE. Keep the time constant of the RC filter well below the minimum on-time pulse width.

Schottky diodes may be necessary on the OUTPUT pin to prevent overshoot and undershoot due to the high impedance to the supply rail and to ground, respectively. A bleeder resistor, placed between the gate and the source of the MOSFET should be used to prevent activating the power switch with extraneous leakage currents during undervoltage lockout.

To prevent noise problems with high-speed switching transients, bypass VREF to ground with a ceramic capacitor close to the IC package. A minimum of 0.1-µF ceramic capacitor is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

11 Layout

11.1 Layout Guidelines

11.1.1 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. Be as direct as possible with the feedback trace and somewhat thick. These two sometimes involve a trade-off, but keeping it away from EMI and other noise sources is the more critical of the two. If possible, run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

11.1.2 Bypass Capacitors

When using a low value ceramic bypass capacitor, it should be located as close to the VCC pin of the device as possible. This eliminates as much trace inductance effects as possible and gives the internal device rail a cleaner voltage supply. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

11.1.3 Compensation Components

For best stability, external compensation components should be placed close to the IC. Keep VFB lead length as short as possible and VFB stray capacitance as small as possible. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to traces with high switching noise.

11.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This also reduces lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.

The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias is required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace needs to conduct a significant amount of current from one plane to the other.

Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

11.2 Layout Example

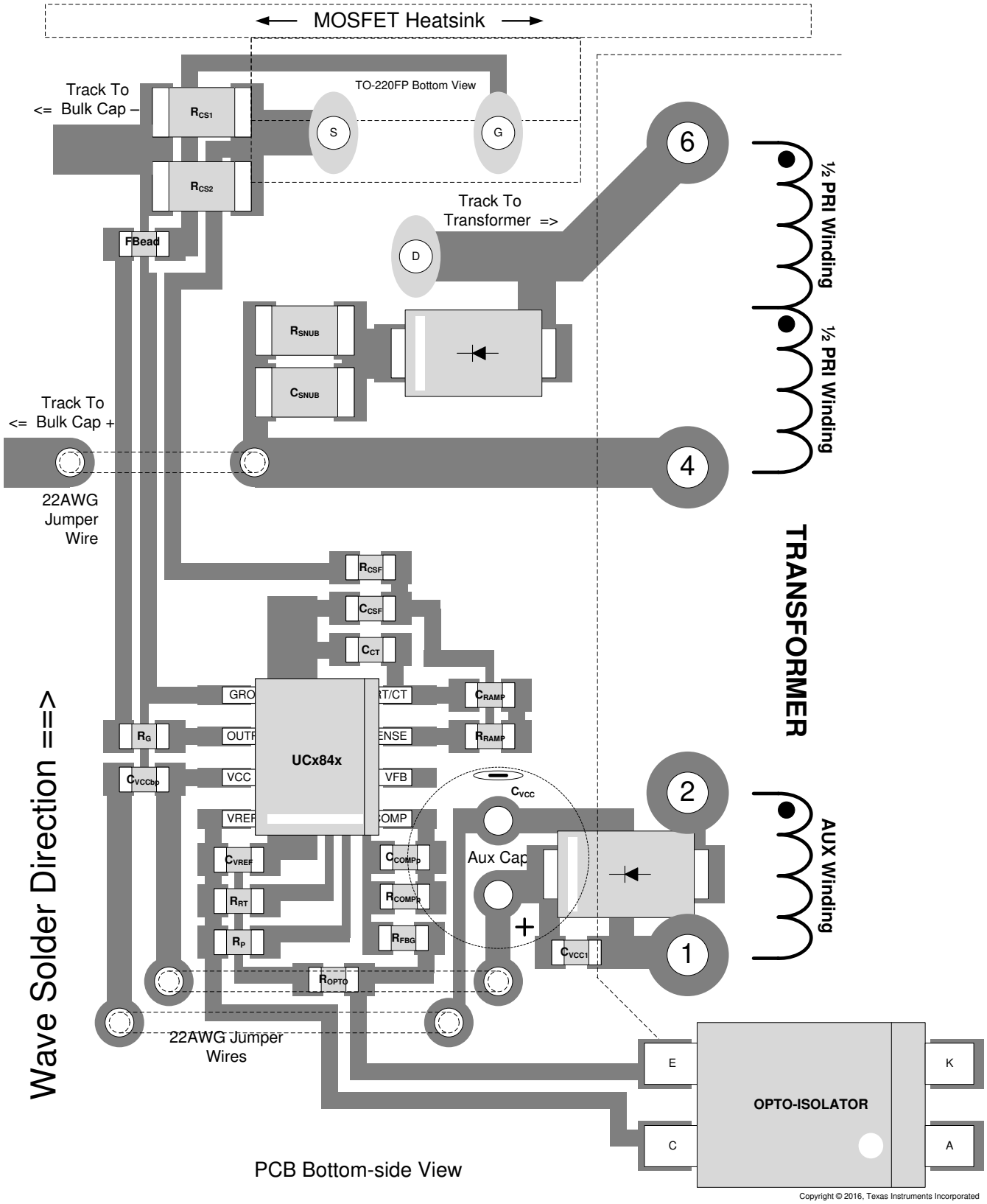


Figure 35. UCx84x Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1842	Click here	Click here	Click here	Click here	Click here
UC2842	Click here	Click here	Click here	Click here	Click here
UC3842	Click here	Click here	Click here	Click here	Click here
UC1843	Click here	Click here	Click here	Click here	Click here
UC2843	Click here	Click here	Click here	Click here	Click here
UC3843	Click here	Click here	Click here	Click here	Click here
UC1844	Click here	Click here	Click here	Click here	Click here
UC2844	Click here	Click here	Click here	Click here	Click here
UC3844	Click here	Click here	Click here	Click here	Click here
UC1845	Click here	Click here	Click here	Click here	Click here
UC2845	Click here	Click here	Click here	Click here	Click here
UC3845	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8670401PA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670401PA UC1842	Samples
5962-8670401VPA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670401VPA UC1842	Samples
5962-8670401XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670401XA UC1842L/ 883B	Samples
5962-8670402PA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670402PA UC1843	Samples
5962-8670402XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670402XA UC1843L/ 883B	Samples
5962-8670403PA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670403PA UC1844	Samples
5962-8670403VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670403VXA UC1844L QMLV	Samples
5962-8670403XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670403XA UC1844L/ 883B	Samples
5962-8670404DA	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type		5962-8670404DA UC1845W/883B	Samples
5962-8670404PA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670404PA UC1845	Samples
5962-8670404VPA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type		8670404VPA UC1845	Samples
5962-8670404VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670404VXA UC1845L QMLV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8670404XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670404XA UC1845L/ 883B	Samples
UC1842J	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1842J	Samples
UC1842J883B	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670401PA UC1842	Samples
UC1842L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670401XA UC1842L/ 883B	Samples
UC1842W	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1842W	Samples
UC1843J	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1843J	Samples
UC1843J883B	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670402PA UC1843	Samples
UC1843L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1843L	Samples
UC1843L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670402XA UC1843L/ 883B	Samples
UC1844J	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1844J	Samples
UC1844J883B	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670403PA UC1844	Samples
UC1844L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670403XA UC1844L/ 883B	Samples
UC1845J	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1845J	Samples
UC1845J883B	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8670404PA UC1845	Samples
UC1845L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1845L	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1845L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670404XA UC1845L/ 883B	Samples
UC1845W	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	UC1845W	Samples
UC1845W883B	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type		5962-8670404DA UC1845W/883B	Samples
UC2842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842D	Samples
UC2842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842	Samples
UC2842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842	Samples
UC2842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842	Samples
UC2842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842D	Samples
UC2842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2842N	Samples
UC2842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2842N	Samples
UC2843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	Samples
UC2843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843	Samples
UC2843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843	Samples
UC2843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843	Samples
UC2843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843	Samples
UC2843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	Samples
UC2843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2843N	Samples
UC2843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2843N	Samples
UC2844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	Samples
UC2844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844	Samples
UC2844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844	Samples
UC2844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844	Samples
UC2844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	Samples
UC2844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	Samples
UC2844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2844N	Samples
UC2844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2844N	Samples
UC2845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	Samples
UC2845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845	Samples
UC2845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845	Samples
UC2845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845	Samples
UC2845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845	Samples
UC2845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	Samples
UC2845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	Samples
UC2845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2845N	Samples
UC2845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2845N	Samples
UC3842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842D	Samples
UC3842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842	Samples
UC3842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842	Samples
UC3842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842D	Samples
UC3842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3842N	Samples
UC3842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3842N	Samples
UC3843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	Samples
UC3843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843	Samples
UC3843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843	Samples
UC3843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843	Samples
UC3843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843	Samples
UC3843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	Samples
UC3843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	Samples
UC3843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3843N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3843N	Samples
UC3844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	Samples
UC3844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844	Samples
UC3844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844	Samples
UC3844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844	Samples
UC3844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	Samples
UC3844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	Samples
UC3844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3844N	Samples
UC3844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3844N	Samples
UC3845AJ	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	0 to 70	UC3845AJ	Samples
UC3845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	Samples
UC3845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845	Samples
UC3845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845	Samples
UC3845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845	Samples
UC3845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845	Samples
UC3845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	Samples
UC3845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	Samples
UC3845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3845N	Samples
UC3845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3845N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1842, UC1842-SP, UC1843, UC1844, UC1844-SP, UC1845, UC1845-SP, UC3842, UC3843, UC3844, UC3845, UC3845AM :

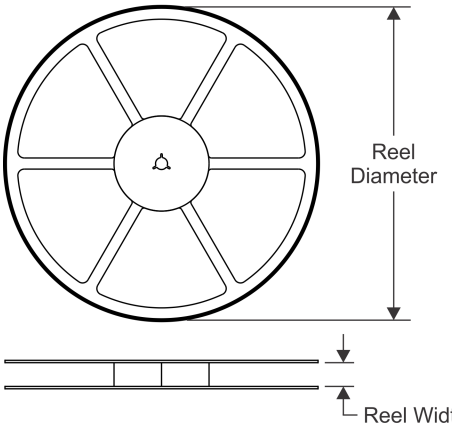
- Catalog: UC3842, UC1842, UC3843, UC3844, UC1844, UC3845, UC1845, UC3842M, UC3845A
- Enhanced Product: UC1845A-EP
- Military: UC1842, UC1843, UC1844, UC1845, UC1845A
- Space: UC1842-SP, UC1843-SP, UC1844-SP, UC1845-SP, UC1845A-SP

NOTE: Qualified Version Definitions:

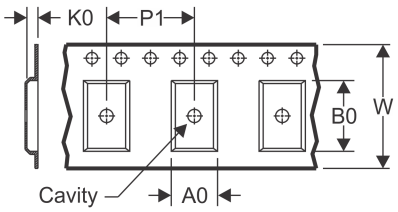
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

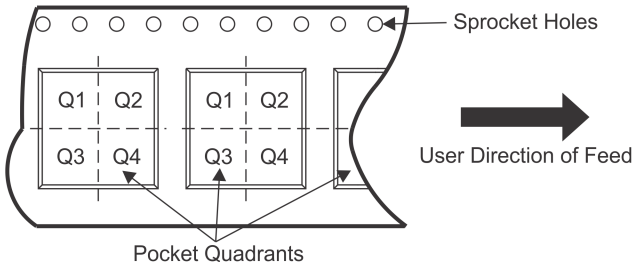


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

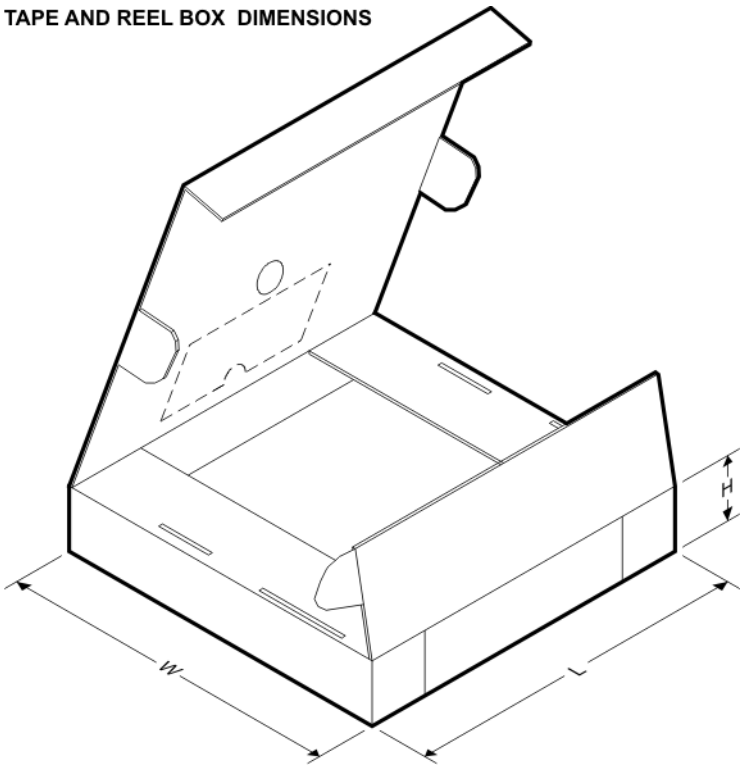
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

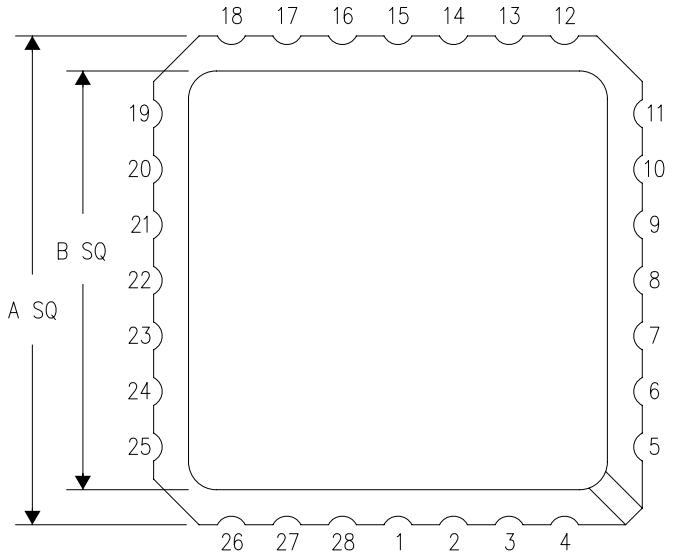


*All dimensions are nominal

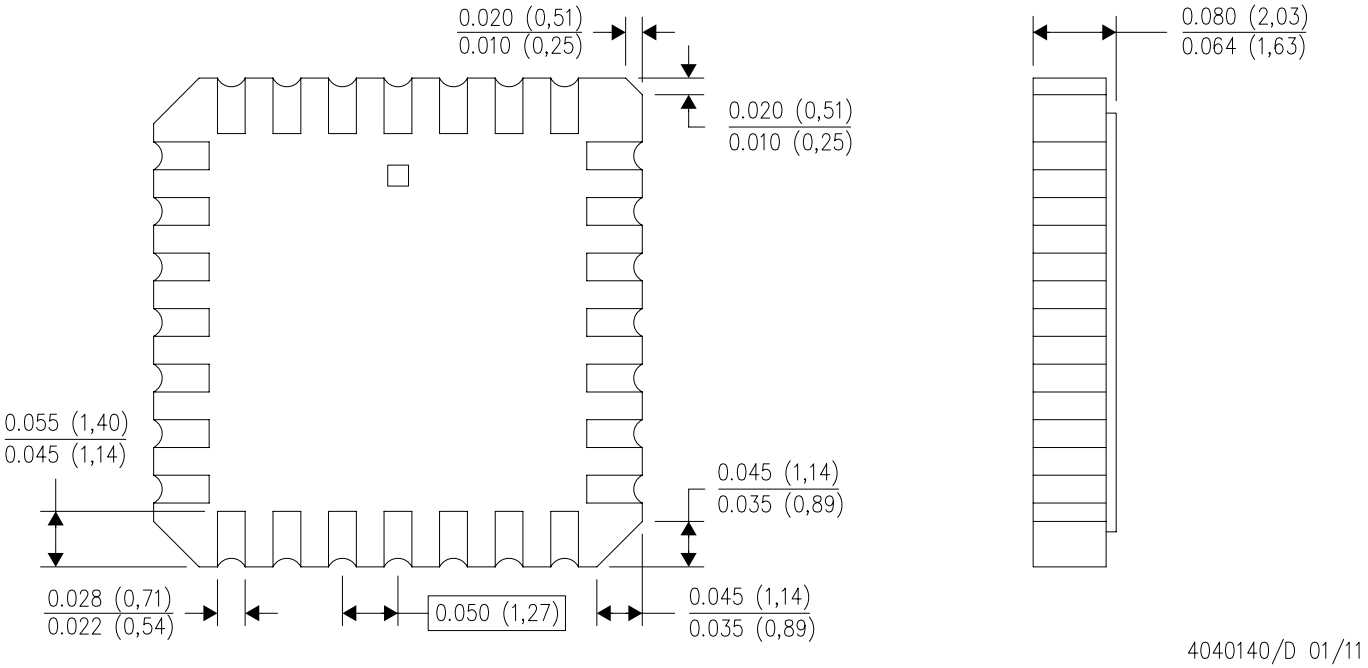
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2845DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3845DTR	SOIC	D	14	2500	333.2	345.9	28.6

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



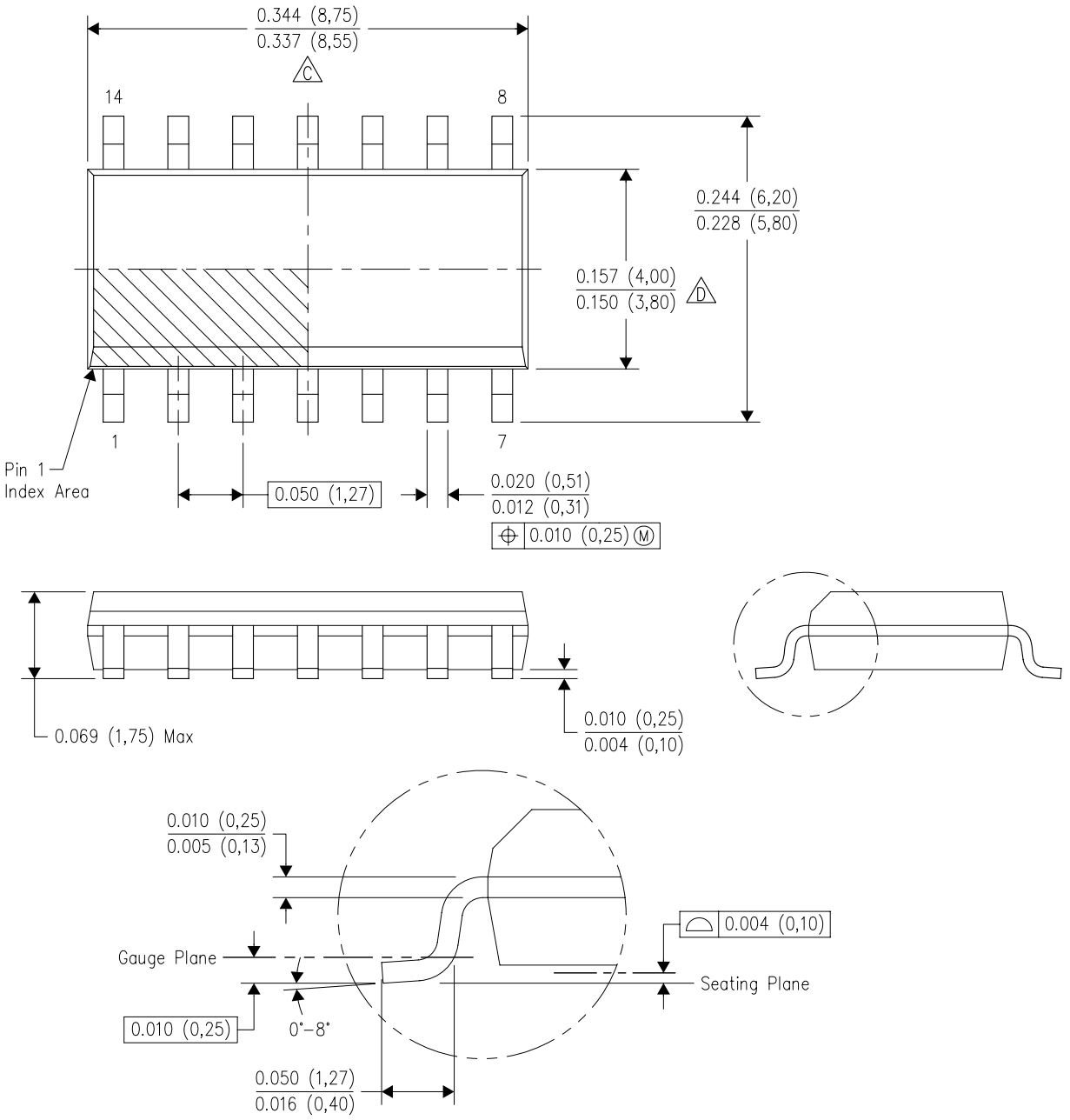
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

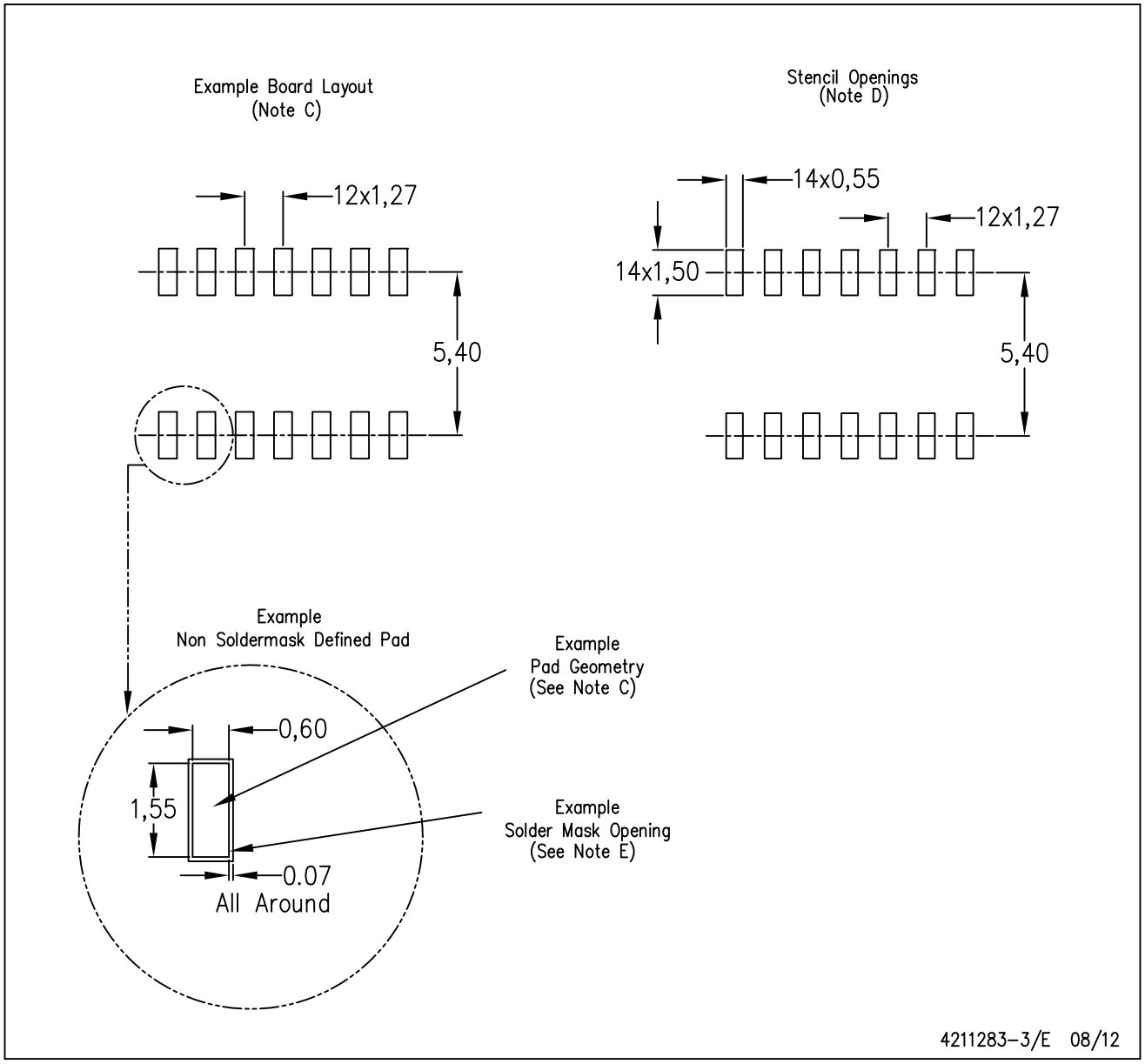
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



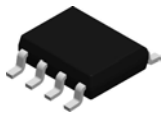
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

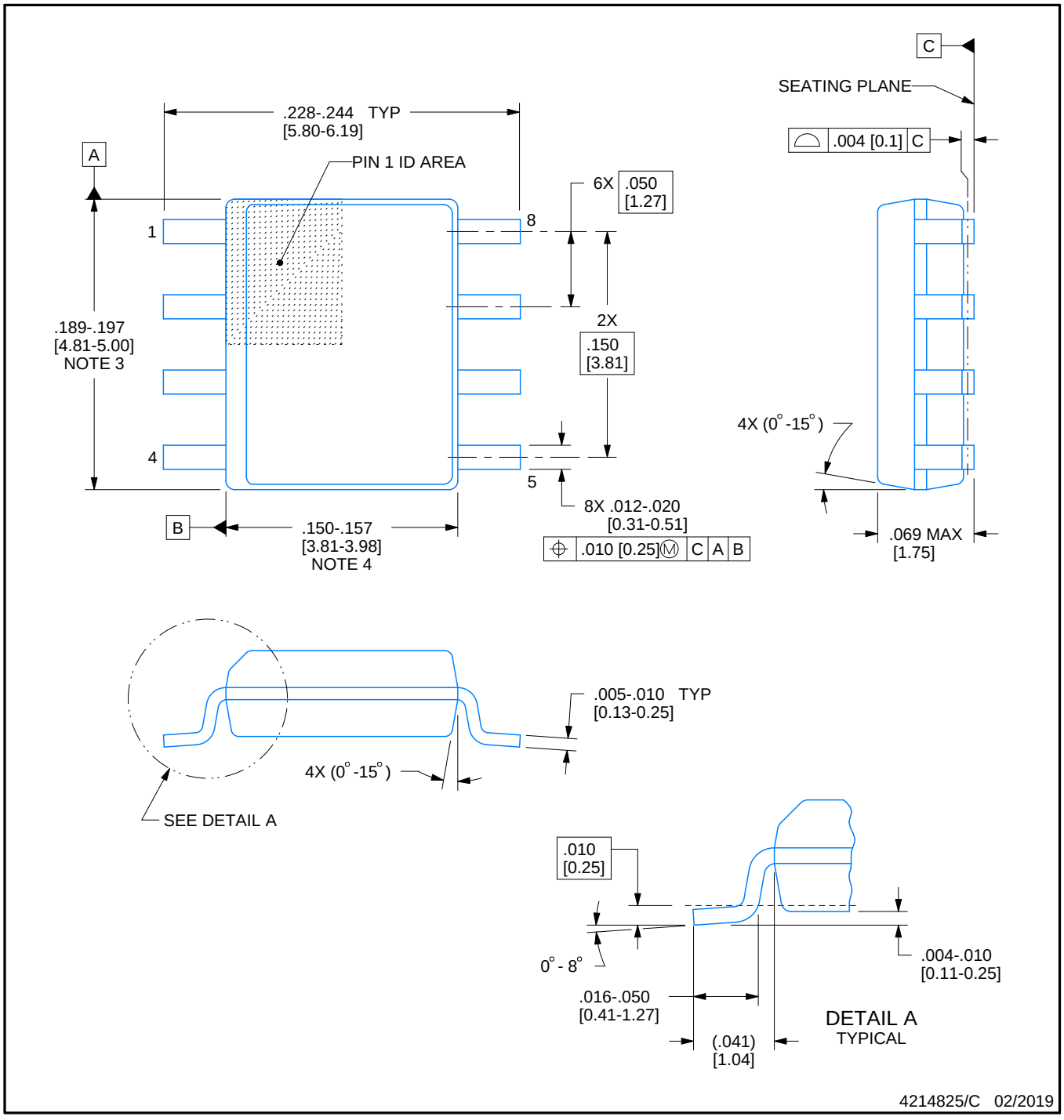


PACKAGE OUTLINE

D0008A

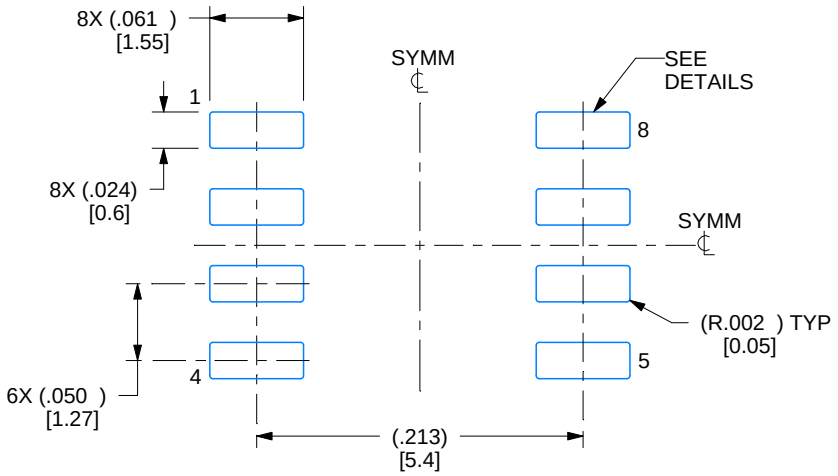
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

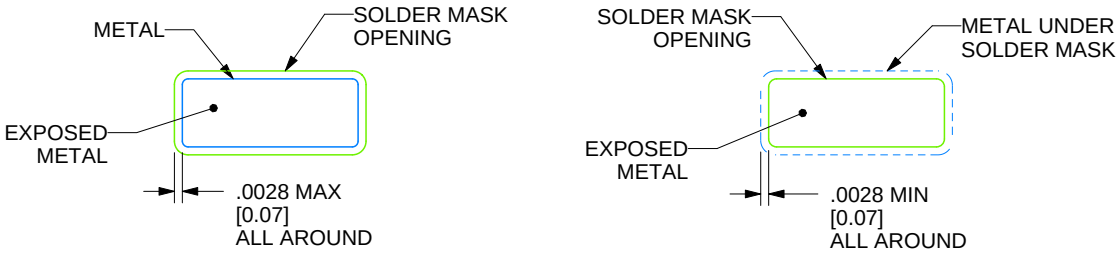


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

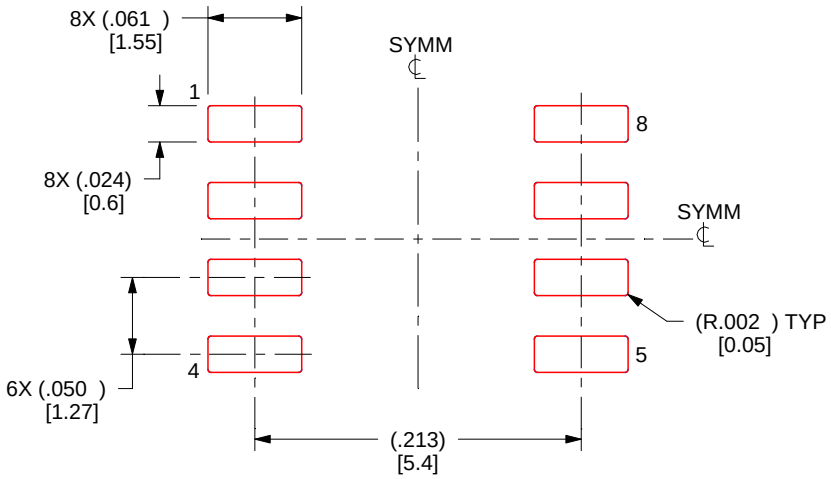
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

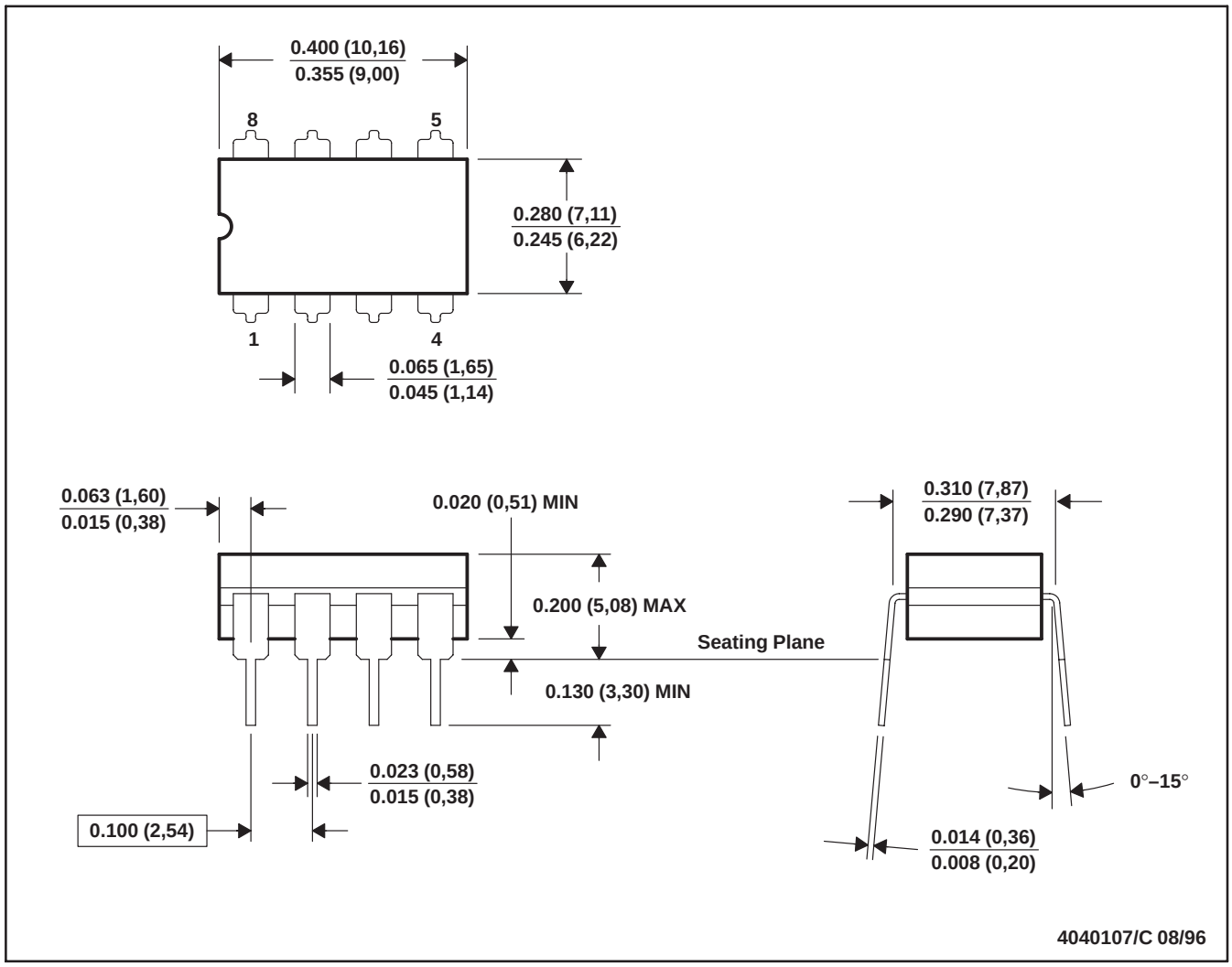
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

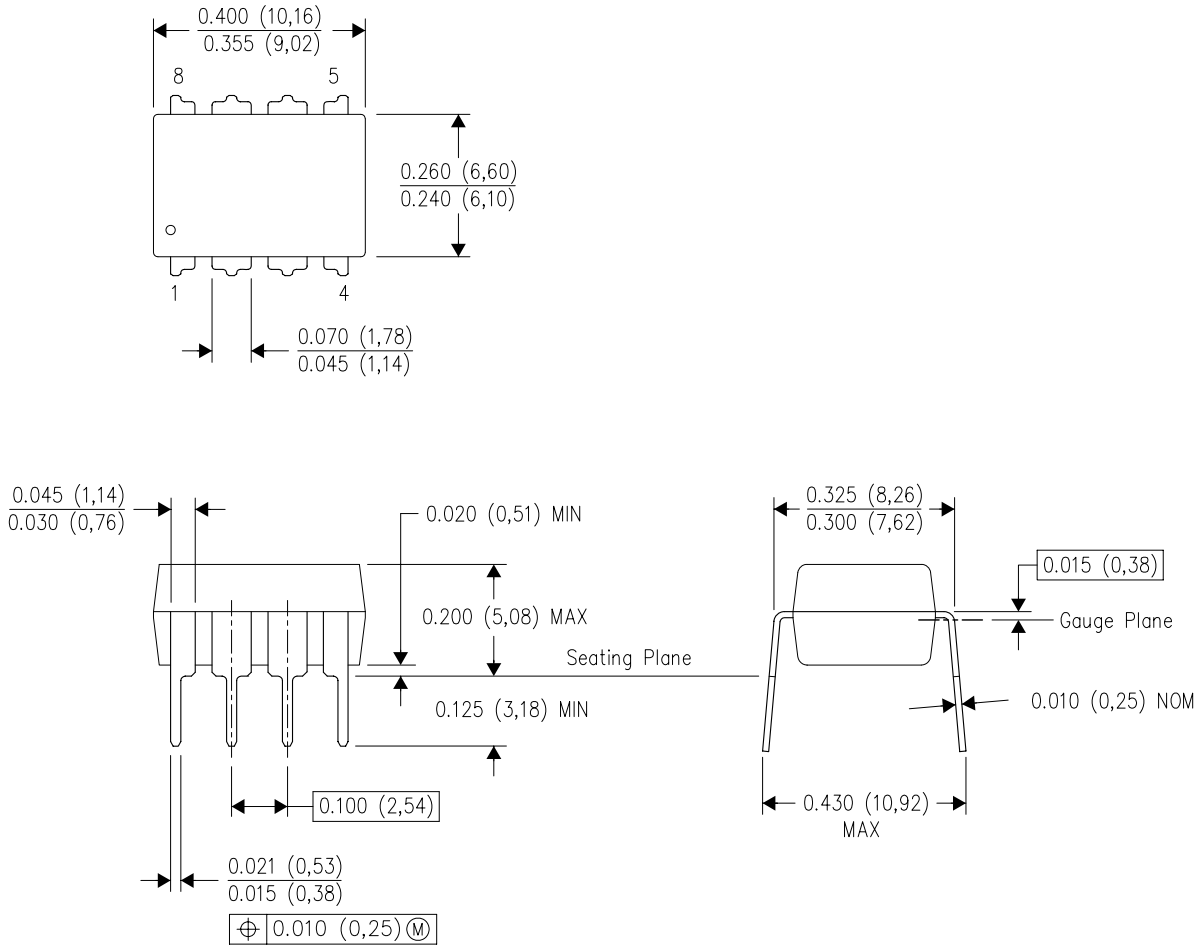
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



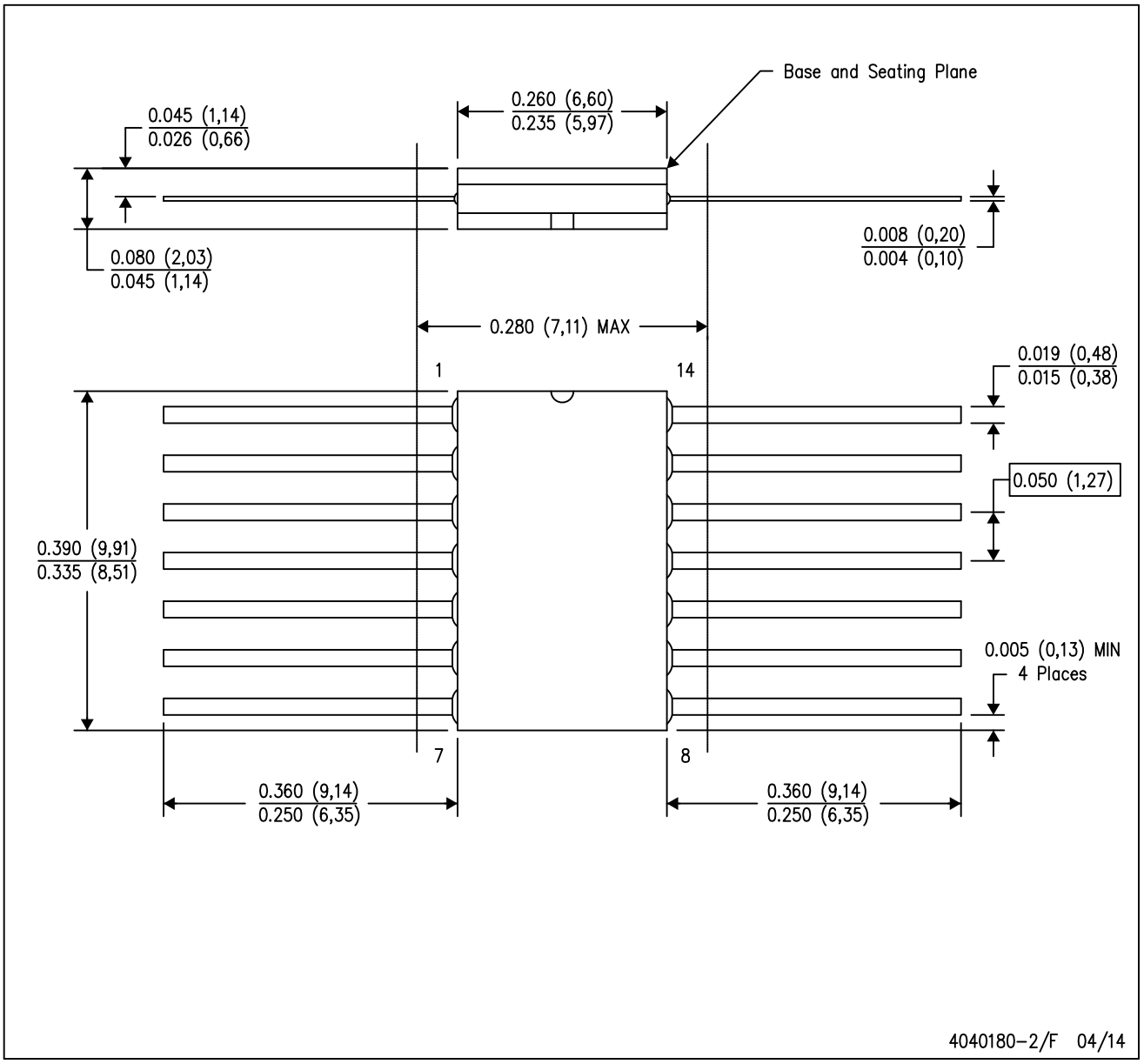
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

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